VTEAM: A General Model for Voltage-Controlled Memristors

Shahar Kvatinsky, *Member, IEEE*, Misbah Ramadan, Eby G. Friedman, *Fellow, IEEE*, and Avinoam Kolodny, *Senior Member, IEEE*

***Abstract*—Memristors are novel electrical devices used for a variety of applications, including memory, logic circuits, and neuromorphic systems. Memristive technologies are attractive due to their nonvolatility, scalability, and compatibility with CMOS. Numerous physical experiments have shown the existence of a threshold voltage in some physical memristors. Additionally, as shown in this brief, some applications require voltage-controlled memristors to operate properly. In this brief, a Voltage ThrEshold Adaptive Memristor (VTEAM) model is proposed to describe the behavior of voltage-controlled memristors. The VTEAM model extends the previously proposed ThrEshold Adaptive Memristor (TEAM) model, which describes current-controlled memristors. The VTEAM model has similar advantages as the TEAM model, i.e., it is simple, general, and flexible, and can characterize different voltage-controlled memristors. The VTEAM model is accurate (below 1.5% in terms of the relative root-mean-square error) and computationally efficient as compared with existing memristor models and experimental results describing different memristive technologies.**

***Index Terms*—MATLAB, memristive systems, memristor, resistive random access memory (ReRAM), resistive switching, SPICE.**

I. Introduction

MEMRISTORS are passive two-port elements with a variable resistance. For ideal memristors, as originally suggested by Chua in 1971 [1], the resistance directly depends on the charge passing through a device or, alternatively, on the integral over time of the applied voltage across a device (i.e., the flux). Memristive devices, which are originally defined by Chua and Kang [2], are an extension of the memristor definition, where the resistance depends on a state variable (or a set of state variables). Although discussions exist in literature concerning the specific definition of memristors [3]–[5], in this brief, the term "memristor" is used to describe both ideal memristors and memristive devices. Emerging nonvolatile memory technologies (e.g., resistive RAM, phase-change memory, and spin-transfer torque magnetoresistance RAM) are considered memristors [4]. Memristors can be also used for other attractive applications, such as logic circuits [24] and neuromorphic systems.

Numerous memristor models have been proposed. Some of the models do not exhibit a threshold [6]–[8]; hence, the resistance of a device changes for any applied voltage (or current). Recently, the ThrEshold Adaptive Memristor (TEAM) model [9] has become widely used due to its simplicity, generality, accuracy, and low computational complexity. The TEAM model relies on a threshold current, where the resistance only changes for currents above a certain level. The experimental data of some memristive devices show, however, the existence of a threshold voltage rather than a threshold current. Furthermore, certain memory and logic applications require memristors with a threshold voltage to operate properly.

Hence, a memristor model with the advantages of the TEAM model (i.e., general, simple, and sufficiently accurate) and exhibiting a threshold voltage is desirable. In this brief, a Voltage TEAM (VTEAM) model, which is a novel memristor model that satisfies these requirements, is presented. The VTEAM model has sufficient accuracy (below 1.5% in terms of the relative RMS error) as compared with existing memristor models and the experimental results of different memristive technologies.

The rest of this brief is organized as follows. The motivation for a threshold voltage and the applicability to various circuits are demonstrated in Section II. In Section III, the VTEAM model is described. A comparison between the VTEAM and previously proposed models and experimental results is presented in Section IV. This brief is summarized in Section V.

II. Motivation for Threshold Voltage

Kvatinsky *et al.* previously proposed the TEAM model [9], which is inspired by the Simmons tunnel barrier model [8]. The TEAM model is based on a threshold current. The resistance of a memristor does not change for currents below a certain threshold current. Experiments on several types of memristive devices, however, have shown the existence of a threshold voltage (e.g., see [6], [18], and [23]), as illustrated in Fig. 1 for different memristors. Furthermore, a memristor with a threshold voltage is more appropriate than a threshold current for certain logic and memory applications, as demonstrated in Section II-A and B for memory and logic, respectively.

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S. Kvatinsky is with the Department of Computer Science, School of Engineering, Stanford University, Stanford, CA 94305 USA (e-mail: shahark@stanfod.edu).

M. Ramadan and A. Kolodny are with the Department of Electrical Engineering, Technion Israel Institute of Technology, Haifa 32000, Israel (e-mail: misba7.90@gmail.com; kolodny@ee.technion.ac.il).

E. G. Friedman is with the Department of Electrical Engineering and Computer Engineering, School of Engineering and Applied Sciences, University of Rochester, Rochester, NY 14627 USA (e-mail: friedman@ece.rochester.edu).

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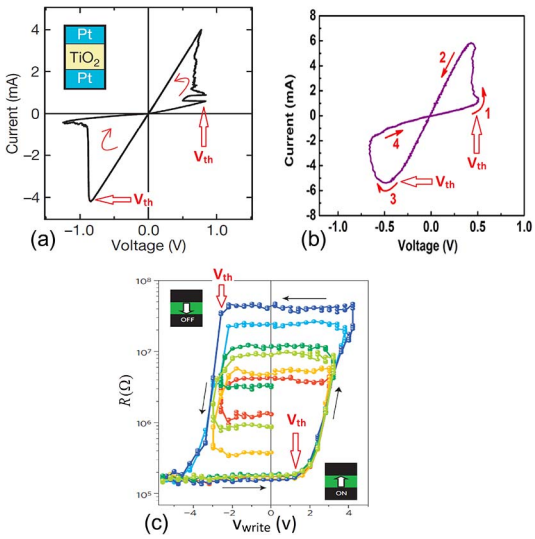


Fig. 1. Current–voltage characteristics of memristors exhibiting a threshold voltage. (a) Pt–TiO_2–Pt memristor [6]. (b) Ag–a-LSMO–Pt memristor [23]. (c) Ferroelectric memristor [18].

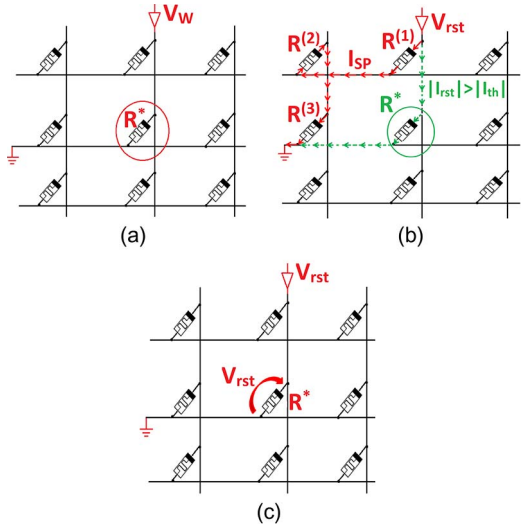
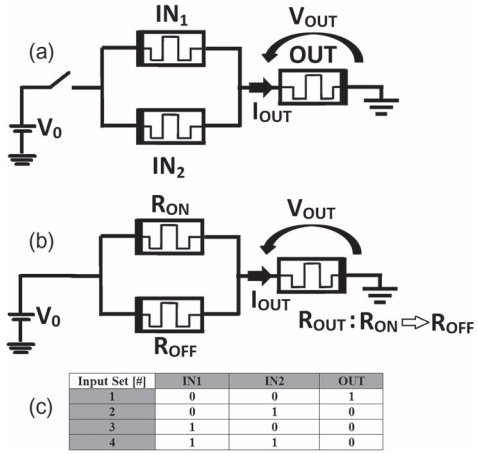


Fig. 2. Illustration of a 3 × 3 memristive crossbar. (a) General write procedure. When the applied voltage V_W is V_{rst} or $V_{\rm set}$, resistance R^* switches to $R_{\rm OFF}$ or $R_{\rm ON}$, respectively. (b) Crossbar with memristors with a threshold current. Applying a constant voltage V_{rst} switches R^* to $R_{\rm OFF}$. The magnitude of current I_{rst} decreases when resistance R^* increases, delaying the transition. Additionally, increasing V_{rst} may cause a partial OFF switching event in the sneak path resistances. (c) Crossbar with memristors with a threshold voltage. The applied voltage $|V_{rst}| > |V_{\rm th}|$ is constant across R^* during switching to $R_{\rm OFF}$.

A. Motivation for Threshold Voltage for Memory

A memristive crossbar is a common memristive memory structure [10]. In a crossbar, as shown in Fig. 2, a write operation is performed by applying a voltage $V_{\rm set}$ or V_{rst} on a selected cell within the crossbar array to write logical one (i.e., low resistance $R_{\rm ON}$) and logical zero (i.e., high resistance $R_{\rm OFF}$), respectively. To write logical zero to a memristor with a threshold current $I_{\rm th}$, the current of the memristor $I(t)$ must be above the threshold current, i.e.,

$$I(t) = \left|\frac{V_{rst}}{R(t)}\right| > |I_{\rm th}| \qquad (1)$$



Input Set [#]	IN1	IN2	OUT
1	0	0	1
2	0	1	0
3	1	0	0
4	1	1	0

Fig. 3. Schematic of the MAGIC NOR gate. (a) Two input memristors IN1 and IN2, and output memristor OUT. The logical operation is achieved by applying a voltage V_0. (b) MAGIC NOR gate illustrating the operation with inputs of IN1 = '1' and IN2 = '0'. (c) NOR truth table.

where $R(t)$ is the resistance of the memristor. During the write operation, $R(t)$ increases, and the current passing through the cell $I(t)$ decreases. The smaller current slows the writing speed. Additionally, for an insufficient write voltage V_{rst}, both performance and reliability issues can occur if (1) is not satisfied. To avoid these issues, higher currents are required, increasing the applied voltage V_{rst}.

High voltages, however, increase power and may lead to a destructive write operation in neighboring cells. For example, in Fig. 2(b), when $|V_{rst}| > |3 \cdot I_{\rm th} \cdot R_{\rm ON}|$ and $R^{(1)} = R^{(2)} = R^{(3)} = R_{\rm ON}$, $|I_{SP}| = (|V_{rst}|/3R_{\rm ON}) > |I_{\rm th}|$ and resistances $R^{(1)}$ and $R^{(3)}$ switch to $R_{\rm OFF}$, creating an undesired partial OFF switching event in some of the neighboring memristors. For memristors with a threshold voltage, however, no performance and reliability issues exist since the applied voltage across each memristor is fixed and since the OFF switching procedure is not affected by the variable resistance, as illustrated in Fig. 2(c).

B. Motivation for Threshold Voltage in Logic Applications

Another example of a memristive circuit that requires a threshold voltage is the memristor-aided logic (MAGIC) NOR gate [11]. A schematic of the MAGIC NOR gate is shown in Fig. 3. In the MAGIC NOR gate, the inputs of the logic gate are the initial resistance of the input memristors (i.e., memristors IN1 and IN2 in Fig. 3), whereas the output memristor (i.e., memristor OUT in Fig. 3) is initialized to logical one (a resistance of $R_{\rm ON}$). The execution of the MAGIC NOR gate is achieved by applying a fixed voltage V_0 to the input memristors. The output of the MAGIC NOR gate is the logical state of the output memristor after the execution, which depends on the current passing through the device or, alternatively, the voltage across the device. The current passing through the output memristor depends on the total resistance of the circuit and consists of the sum of the resistance of the two input memristors connected in parallel and the output memristor.

For a correct logical behavior, the resistance of the output memristor does not change when both inputs are logical zero (i.e., the resistance of the circuit is 1.5 $R_{\rm OFF}$), and it changes for any other input set [as shown in Fig. 3(c)]. Specifically, when one input of the gate is logical zero (a resistance of $R_{\rm OFF}$)

and the other input is logical one ($R_{\rm ON}$, where $R_{\rm OFF} \gg R_{\rm ON}$), the resistance of the output memristor changes when switching from $R_{\rm ON}$ to $R_{\rm OFF}$. Assume a memristor with current thresholds of $|i_{\rm ON}| = i_{\rm OFF} = 20\ \mu$A and circuit parameters of $R_{\rm ON} = 1$ kΩ, $R_{\rm OFF} = 100$ kΩ, and $V_0 = 1$ V. The current passing through the output memristor is

$$I_{\rm OUT}(t) = \frac{V_0}{(R_{\rm ON} \| R_{\rm OFF}) + R_{\rm OUT}(t)} \approx \frac{V_0}{R_{\rm ON} + R_{\rm OUT}(t)} \geq I_{\rm th} \tag{2}$$

where $R_{\rm OUT}(t)$ is the resistance of the output memristor, which increases from the initial value of $R_{\rm ON}$. The current is reduced until a current threshold is exceeded and remains constant, as illustrated in Fig. 3(b). For this numerical example, $R_{\rm OUT} = 49$ k$\Omega < (R_{\rm OFF}/2)$, which is considered logical one, producing an incorrect output.

For a memristor with a threshold voltage, however, full switching to $R_{\rm OFF}$ is achieved. $V_{\rm OUT}$, i.e., the voltage at the output memristor, as shown in Fig. 3, is

$$\begin{aligned} V_{\rm OUT}(t) &= V_0 \cdot \frac{R_{\rm OUT}(t)}{R_{\rm OUT}(t) + (R_{\rm ON} \| R_{\rm OFF})} \\ &\approx V_0 \cdot \frac{R_{\rm OUT}(t)}{R_{\rm OUT}(t) + R_{\rm ON}}. \end{aligned} \tag{3}$$

For a proper operation (i.e., switching to logical zero), the applied voltage V_0 must exceed the threshold voltage during the entire operation. From (3), $V_{\rm OUT}$ increases as $R_{\rm OUT}$ increases; hence, a complete switch to $R_{\rm OFF}$ is achieved for memristors with a threshold voltage. A proper MAGIC operation with the proposed memristor model was presented in [11].

III. VTEAM

The VTEAM model is described in this section. Similar to the predecessor model (the TEAM model [9]), the VTEAM model is based on an expression of the derivative of an internal state variable. The VTEAM model combines the advantages of the TEAM model (i.e., simple, general, accurate, and designer friendly) with a threshold voltage rather than a threshold current. The current–voltage relationship of the VTEAM model is undefined and can be freely chosen from any current–voltage characteristics. Several examples of possible current–voltage relationships are described in this section. Generally, a voltage-controlled time-invariant memristive device [2] is represented by

$$\frac{dw}{dt} = f(w, v) \tag{4}$$

$$i(t) = G(w, v) \cdot v(t) \tag{5}$$

where w is an internal state variable, $v(t)$ is the voltage across the memristive device, $i(t)$ is the current passing through the memristive device, $G(w, v)$ is the device conductance, and t is time. Note that $f(w, v)$ is a general function of the derivative of state variable w. Specifically, these expressions allow the existence of a threshold voltage.

Analogous to the derivative of the state variable in the TEAM model, the derivative of the state variable [the realization of (4)] in the VTEAM model is

$$\frac{dw(t)}{dt} = \begin{cases} k_{\rm off} \cdot \left(\frac{v(t)}{v_{\rm off}} - 1\right)^{\alpha_{\rm off}} \cdot f_{\rm off}(w), & 0 < v_{\rm off} < v \quad \text{(6a)} \\ 0, & v_{\rm on} < v < v_{\rm off} \quad \text{(6b)} \\ k_{\rm on} \cdot \left(\frac{v(t)}{v_{\rm on}} - 1\right)^{\alpha_{\rm on}} \cdot f_{\rm on}(w), & v < v_{\rm on} < 0 \quad \text{(6c)} \end{cases}$$

where $k_{\rm off}$, $k_{\rm on}$, $\alpha_{\rm off}$, and $\alpha_{\rm on}$ are constants, and $v_{\rm on}$ and $v_{\rm off}$ are threshold voltages. Parameter $k_{\rm off}$ is a positive number, whereas $k_{\rm on}$ is a negative number. Functions $f_{\rm off}(w)$ and $f_{\rm on}(w)$ represent the dependence of the derivative of the state variable on state variable w. These functions behave as window functions, which constrain the state variable to bounds of $w \in [w_{\rm on}, w_{\rm off}]$. Nevertheless, different window functions can be used, e.g., the window functions [9], [12]–[14] or perhaps an ideal rectangular window function where the derivative of w is zero when $w \notin (w_{\rm on}, w_{\rm off})$.

The current–voltage relationship and $G(w, v)$ are not inherently defined in the VTEAM model. A linear dependence of the resistance and the state variable can be achieved, where the current–voltage relationship is

$$i(t) = \left[R_{\rm ON} + \frac{R_{\rm OFF} - R_{\rm ON}}{w_{\rm off} - w_{\rm on}} \cdot (w - w_{\rm on})\right]^{-1} \cdot v(t) \tag{7}$$

where $w_{\rm on}$ and $w_{\rm off}$ are the bounds of internal state variable w, and $R_{\rm ON}$ and $R_{\rm OFF}$ are the corresponding resistances of the device when the state variable is $w_{\rm on}$ and $w_{\rm off}$, respectively. Alternatively, exponential dependence on the state variable can be assumed, as in [8]. In this case, the current–voltage relationship is

$$i(t) = \frac{e^{-\frac{\lambda}{w_{\rm off} - w_{\rm on}} \cdot (w - w_{\rm on})}}{R_{\rm ON}} \cdot v(t) \tag{8}$$

where λ is a fitting parameter, and $e^{\lambda} = (R_{\rm OFF}/R_{\rm ON})$.

IV. Fitting VTEAM to Other Memristor Models and Experimental Data

The VTEAM model is a general model that can be fit to numerous memristor models and experimental data due to its inherent generality and robustness. Given the current–voltage characteristics of a specific memristor, a set of parameters is chosen to fit the VTEAM model to a reference I–V relationship. To fit the I–V curve, the relative RMS error is minimized using gradient descent [15] and simulated annealing algorithms [16]. The relative RMS error is

$$e_{i,v} = \sqrt{\frac{1}{N} \cdot \left(\frac{\sum_{i=1}^{N} (V_{{\rm VTEAM},i} - V_{{\rm ref},i})^2}{\bar{V}_{\rm ref}^2} + \frac{\sum_{i=1}^{N} (I_{{\rm VTEAM},i} - I_{{\rm ref},i})^2}{\bar{I}_{\rm ref}^2} \right)} \tag{9}$$

where N is the number of samples; $V_{{\rm VTEAM},i}$ and $I_{{\rm VTEAM},i}$ are the corresponding ith sample of the voltage and current of the VTEAM model, respectively; $V_{{\rm ref},i}$ and $I_{{\rm ref},i}$ are the corresponding ith sample of the voltage and current of the reference model, respectively; and $\bar{V}_{\rm ref}$ and $\bar{I}_{\rm ref}$ are the Euclidean norm of the voltage and current of the reference model, respectively.

The fitting procedure is iterated on $k_{\rm off}$ and $k_{\rm on}$ to minimize the error function given in (9). To avoid convergence to a local minimum rather than the optimal global fitting, the remaining fitting parameters (i.e., $\alpha_{\rm off}$, $\alpha_{\rm on}$, $v_{\rm off}$, $v_{\rm on}$, $R_{\rm OFF}$, and $R_{\rm ON}$) are manually chosen to exhibit a similarity (a relative RMS error

TABLE I
FITTING CHARACTERISTICS OF THE VTEAM MODEL TO EXPERIMENTAL MEMRISTIVE DEVICES

Physical device		Pt-Hf-Ti memristor [17]	Ferroelectric memristor [18]	Metallic nanowire memristor [19]
Optimized parameters of the VTEAM model	α_{off}	1	5	3
	α_{on}	3	5	9
	v_{off} [v]	0.5	1.4	0.145
	v_{on} [v]	-0.53	-5.7	-0.09
	R_{OFF} [Ω]	$2.5\cdot10^{3}$	$5\cdot10^{7}$	34
	R_{ON} [Ω]	100	$1.5\cdot10^{5}$	17.3
	k_{off} [m/s]	$4.03\cdot10^{-8}$	10^{-4}	$5\cdot10^{-4}$
	k_{on} [m/s]	-80	-30	$-1.32\cdot10^{-6}$
	w_{off} [nm]	10	10	10
	w_{on} [nm]	0	0	0
	w_{init} [nm]	10	0	0
	i-v	linear	linear	exponent
$e_{v,i}$ minimal value achieved		1.12%	1.48%	0.41%

below 1.5%) to the reference I–V relationship. Furthermore, an ideal window function is used for the VTEAM model during the fitting procedure to bound the state variable, and the current–voltage relationship is chosen to be the original I–V relationship of the reference model. Fitting the VTEAM model to experimental data is presented in the following section, followed by fitting and a comparison with other memristor models in Section IV-B.

A. VTEAM Model Versus Experimental Data

In this section, three physical memristive devices are compared with the VTEAM model, i.e., a Pt–Hf–Ti memristor where the active switching layer has been prepared in the same manner as reported in [17], a ferroelectric memristor [18], and a single-component metallic nanowire memristor [19]. The resulting parameters are listed in Table I, and the graphical results of the I–V relationship are depicted in Fig. 4.

B. VTEAM Model Versus Previously Proposed Models

Previously proposed memristor models, such as the Yakopcic [20] and boundary condition memristor (BCM) [21] models, also exhibit a threshold voltage. Both models, however, operate according to a different state variable mechanism than the VTEAM model. The VTEAM model increases the resistance while moving state variable w toward boundary $w_{\rm off}$. In the Yakopcic and BCM models, however, increasing the state variable decreases the resistance of the device. Although this difference is only based on a different definition and terminology, to accurately compare these models with the VTEAM model, a modification of the original models is required. The I–V relationship of both models is mirrored according to the V plane and the I plane, i.e., the opposite polarity of the voltage and the current are used, or alternatively in circuit terms, the memristor is connected to the opposite polarity. The fit of the VTEAM model to the Yakopcic, BCM, and TEAM models is listed in Table II. In Fig. 5, a graphical description of the I–V relationship is shown.

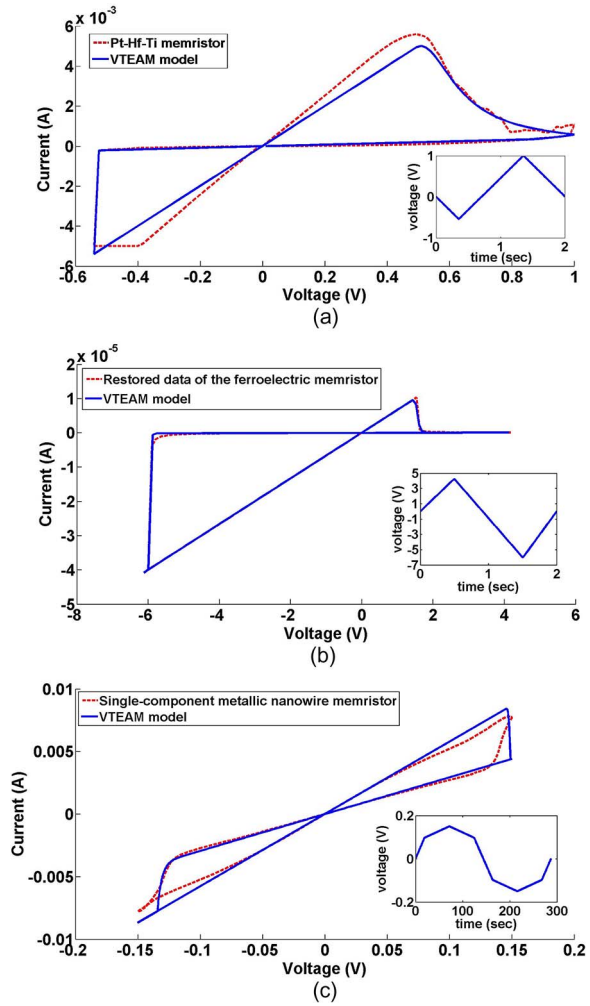


Fig. 4. VTEAM model fit to experimental results. The VTEAM model is fitted to a (a) Pt–Hf–Ti memristor [17], (b) a ferroelectric memristor [18], and a (c) single-component metallic nanowire memristor [19]. The applied voltages across the devices are shown in the subwindow.

TABLE II
FITTING CHARACTERISTICS OF THE VTEAM MODEL TO OTHER MEMRISTOR MODELS

Memristor model		Yakopcic [20]	BCM [21]	TEAM [9]
Optimized parameters of the VTEAM model	α_{off}	3	1	1
	α_{on}	3	1	3
	v_{off} [v]	0.16	0.15	0.02
	v_{on} [v]	-0.15	-3.5	-0.2
	R_{OFF} [Ω]	1069.5	10^{4}	10^{3}
	R_{ON} [Ω]	387	10^{3}	50
	k_{off} [m/s]	$2.49\cdot10^{-6}$	$5.46\cdot10^{-10}$	$5\cdot10^{-4}$
	k_{on} [m/s]	$-2.2\cdot10^{-4}$	$-7.34\cdot10^{-8}$	-10
	w_{off} [nm]	10	10	3
	w_{on} [nm]	0	0	0
	w_{init} [nm]	8.9	7.7778	0
	i-v relationship	linear	linear	linear
$e_{v,i}$ minimal value achieved		0.43%	0.09%	0.44%

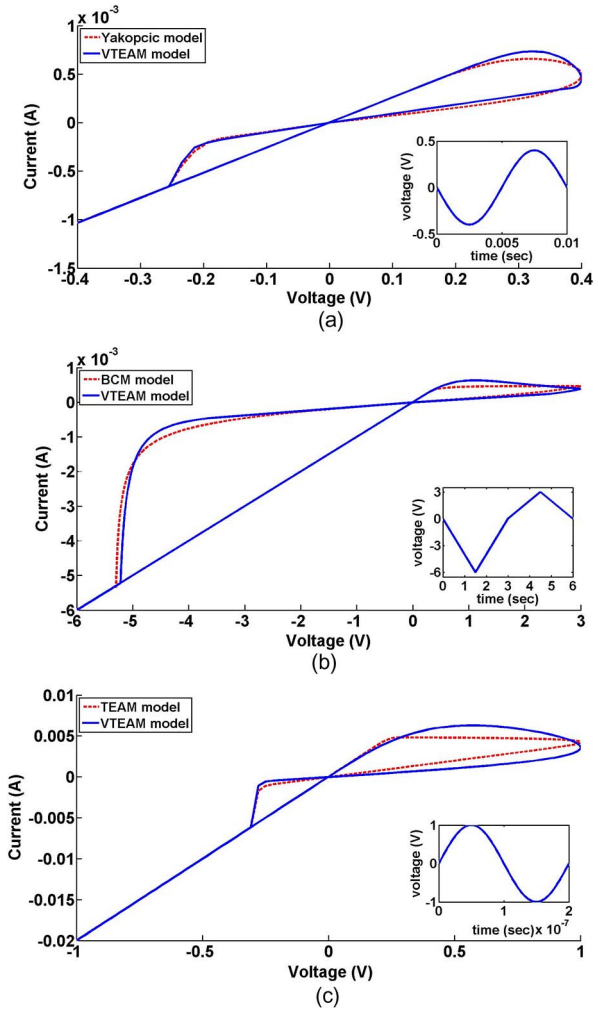


Fig. 5. Comparison of the VTEAM model with previously proposed memristor models. (a) Yakopcic model [20]. (b) BCM model [21]. (c) TEAM model [9].

V. Conclusion

A memristor model that exhibits a threshold voltage is required to accurately characterize physical behavior and to apply to several memory and logic circuits. In this brief, the VTEAM model has been presented, which is a model that exhibits a threshold voltage. The proposed model has the advantages of the TEAM model (i.e., flexibility, generality, and sufficient accuracy).

A comparison between the VTEAM model and experimental data is provided. The sufficient accuracy of the VTEAM model as compared with the experimental data is achieved by tuning the fitting parameters, demonstrating generality and flexibility. The VTEAM model also exhibits sufficient accuracy while fitting to previously proposed memristor models with a threshold voltage. These models lack the generality of the VTEAM model and cannot be fit to the experimental data.

The VTEAM and TEAM models exhibit a threshold voltage and a threshold current, respectively. Together, these models are applicable to a variety of memristive technologies. These models have been implemented in Verilog-A for SPICE simulations [22], and they can be used to design memristive circuits.

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