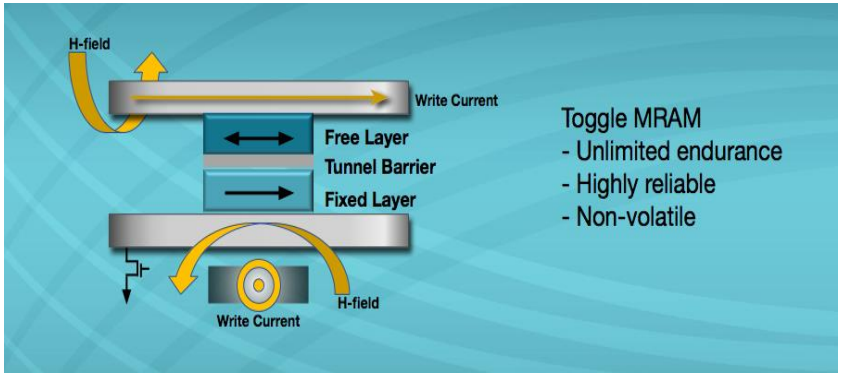
ASIC² Project:
MRAM Versus SRAM
Design of a non-volatile FIFO based on MRAM

***Background**: Toggle MRAM uses a 1 transistor, 1 MTJ cell to provide a simple, high-density memory. Everspin uses a patented Toggle cell design that delivers high reliability. Data are always non-volatile for 20-years at temperature. During a read, the pass transistor is activated and data is read by comparing the resistance of the cell to a reference device. During writes, the magnetic field from Write Line 1 and Write Line 2 writes the cell at the intersection of the two lines but does not disturb other cells on either line. MRAM products employ a one transistor, one magnetic tunnel junction (MTJ) memory cell for the storage element. The MTJ is composed of a fixed magnetic layer, a thin dielectric tunnel barrier and a free magnetic layer. When a bias is applied to the MTJ, electrons that are spin polarized by the magnetic layers traverse the dielectric barrier through a process known as tunneling.*

Project Description:

- Study the theory of Magnetic RAM and its interface
- Write an interface on FPGA to standard SRAM 35nsec
- Make a circuit including a MRAM and a SRAM
- Connect the circuit to the FPGA and debug the interface with SRAM
- Compare SRAM and MRAM performances
- Write a FIFO interface for the MRAM and demonstrate functionality
- Propose a MRAM application and develop it on the FPGA Board



Prerequisites: **TBD**

Recommended: TBD

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