MRL – Memristor Ratioed Logic

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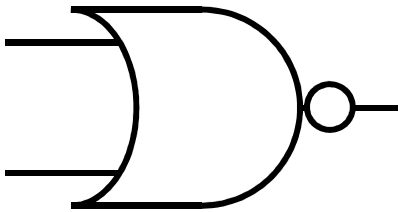
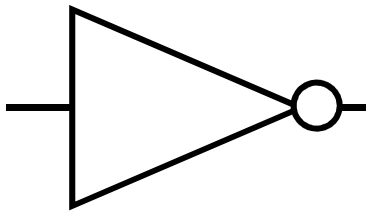
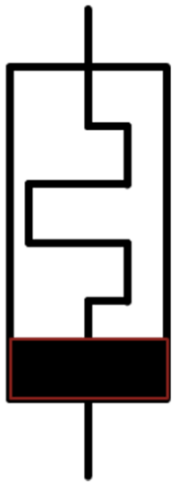
Memristors are Useful for Logic

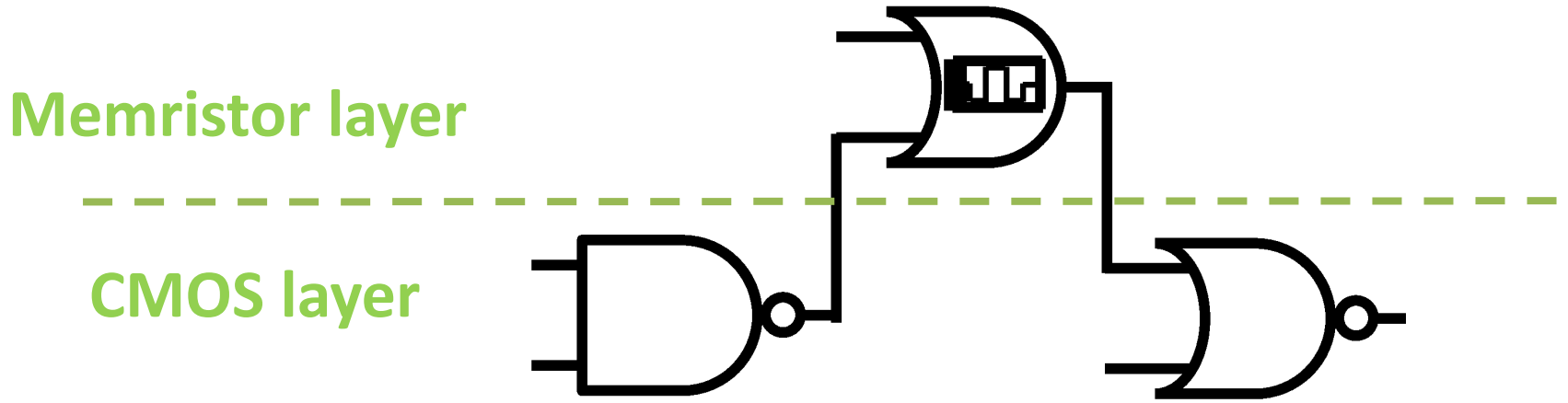
- Memristors are useful not only for memory
- This talk is about **memristor-based logic circuits**







Why Use Memristors in Logic?



Integrating memristors with standard logic

Saves die area

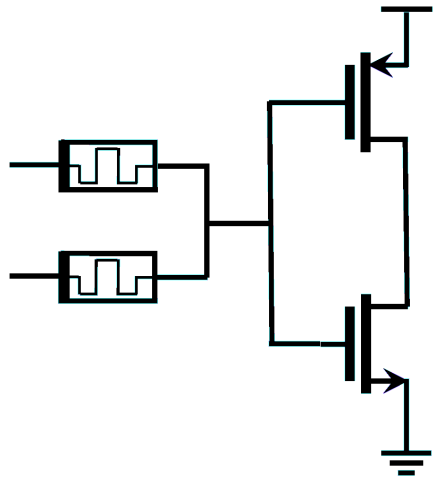
More logic on die

Our Contribution

- MRL – Memristor **Ratioed Logic** –

  a new hybrid CMOS-memristor logic family

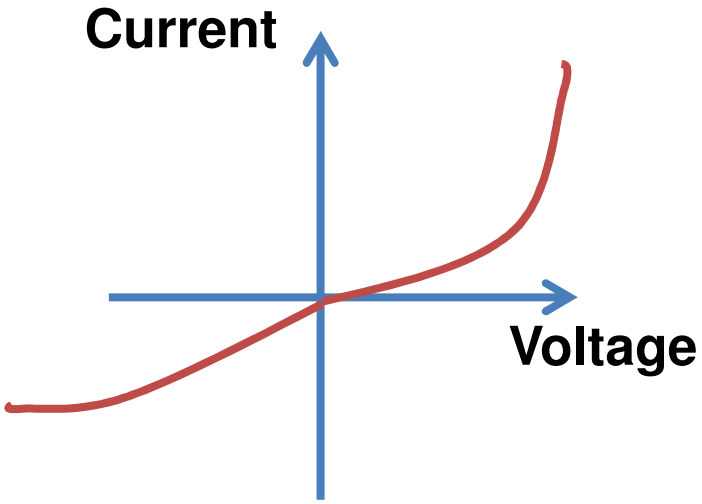
- An eight-bit full adder case study



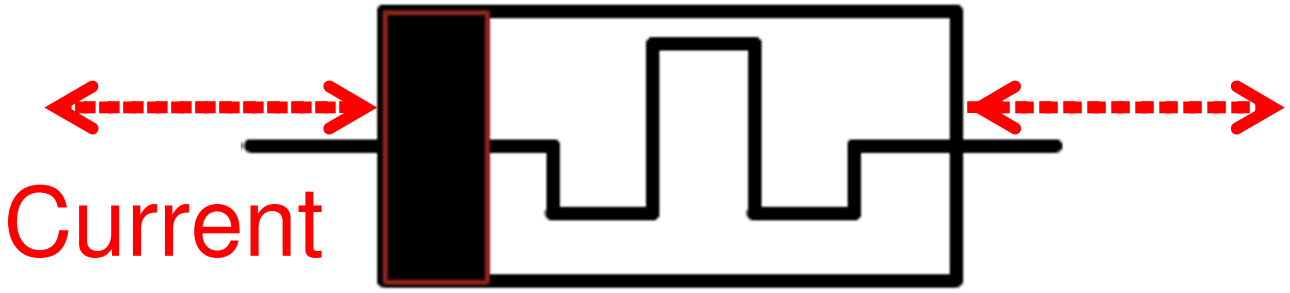
Outline

- Motivation / Why logic with memristors?
- **MRL – Memristor Ratioed Logic**
- Eight bit full adder case study
- Additional Issues
- Conclusions

Memristor Polarity

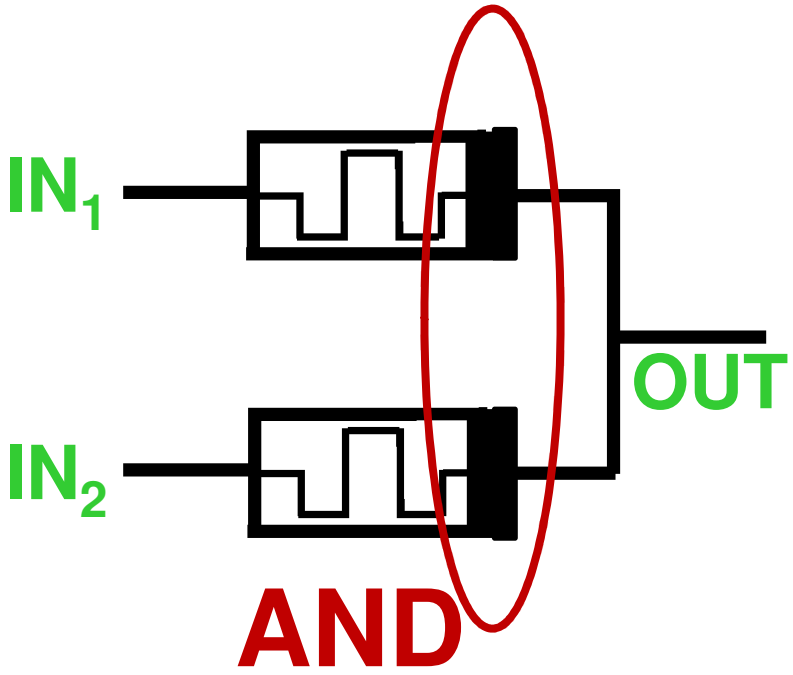


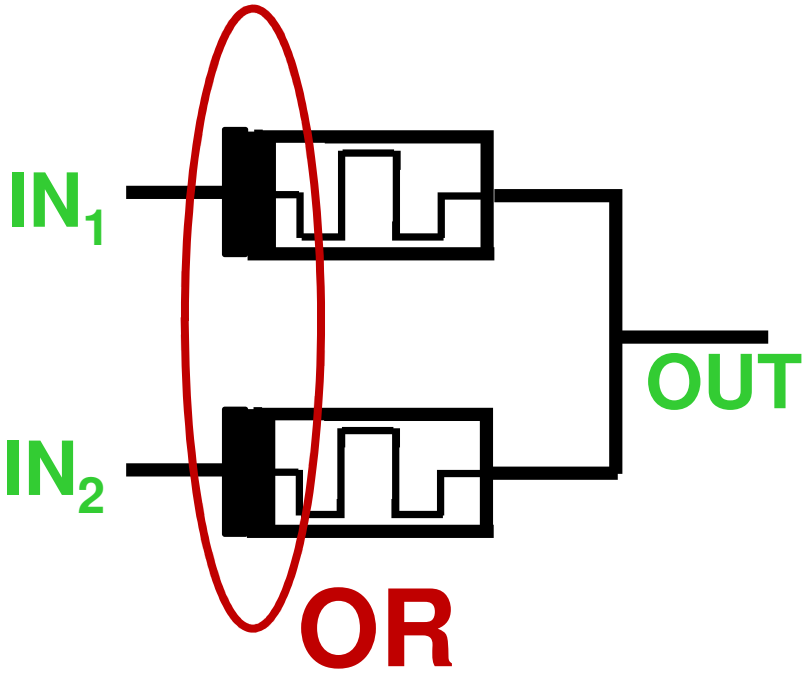
Decrease resistance



MRL - AND and OR

- Voltage as logic state
- Memristors are used as computational elements



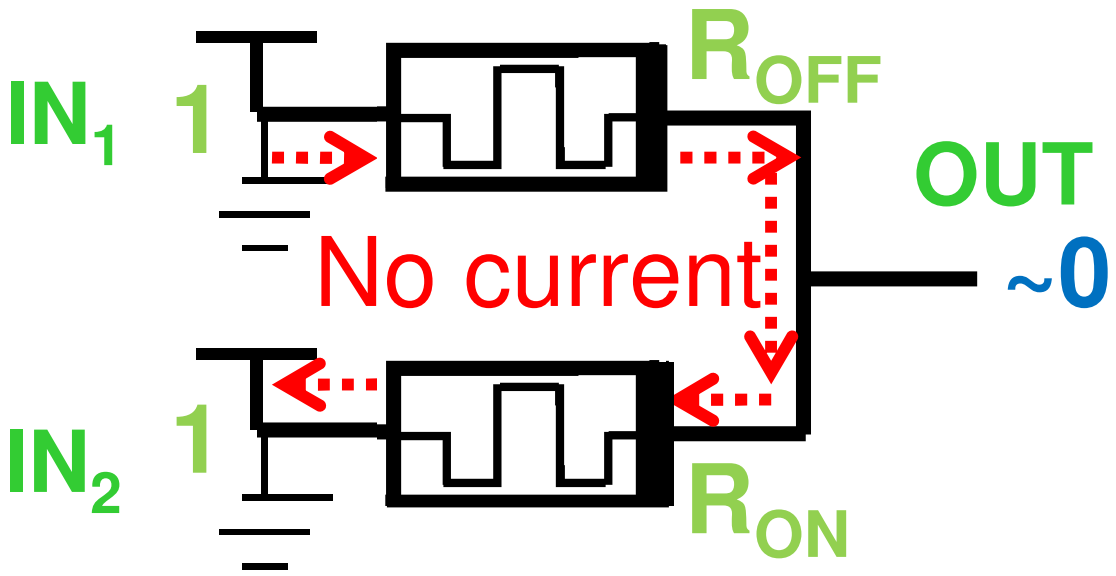


AND Operation

$$V_{OUT} = V_{CC} \cdot \frac{R_{ON}}{R_{ON} + R_{OFF}} \approx V_{CC} \cdot \frac{R_{ON}}{R_{OFF}} << V_{CC}$$

IN_1	IN_2	AND
0	0	0
0	1	0
1	0	0
1	1	1

Increase resistance

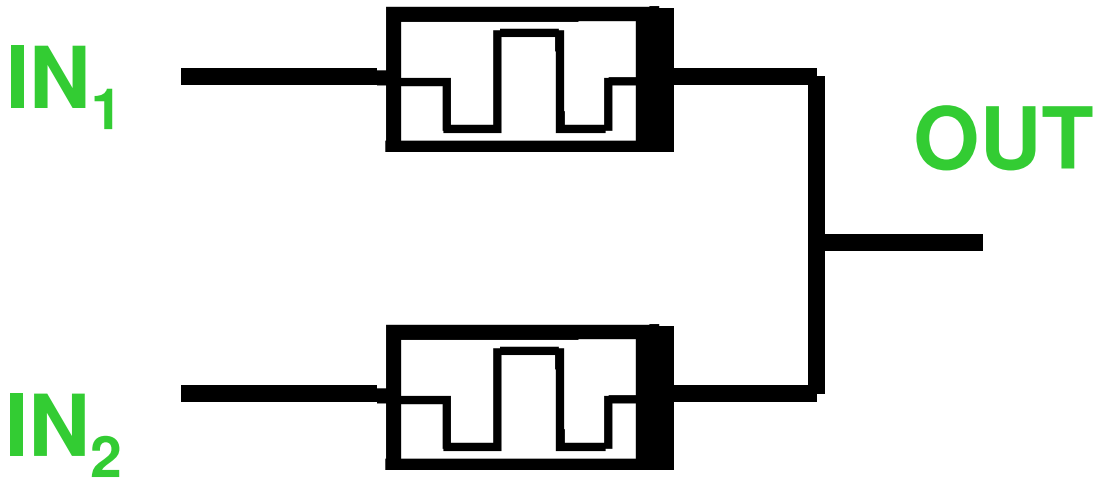


Decrease resistance

$R_{OFF} >> R_{ON}$

AND to OR

IN_1	IN_2	OR
0	0	0
0	1	1
1	0	1
1	1	1



A OR B

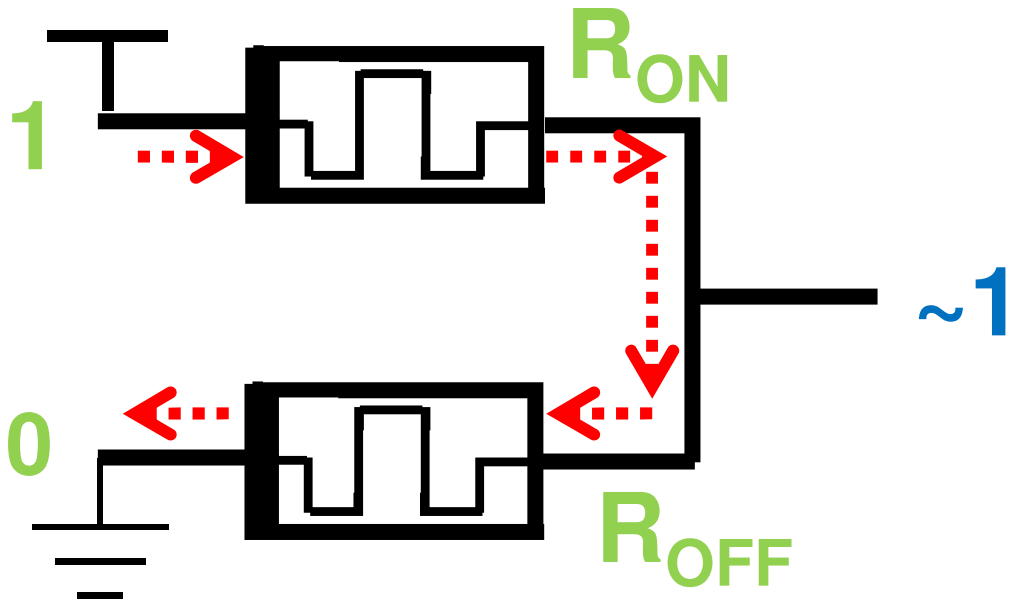
OR Operation

$$V_{OUT} = V_{CC} \cdot \frac{R_{OFF}}{R_{ON} + R_{OFF}} \approx V_{CC}$$

$R_{OFF} >> R_{ON}$

IN_1	IN_2	OR
0	0	0
0	1	1
1	0	1
1	1	1

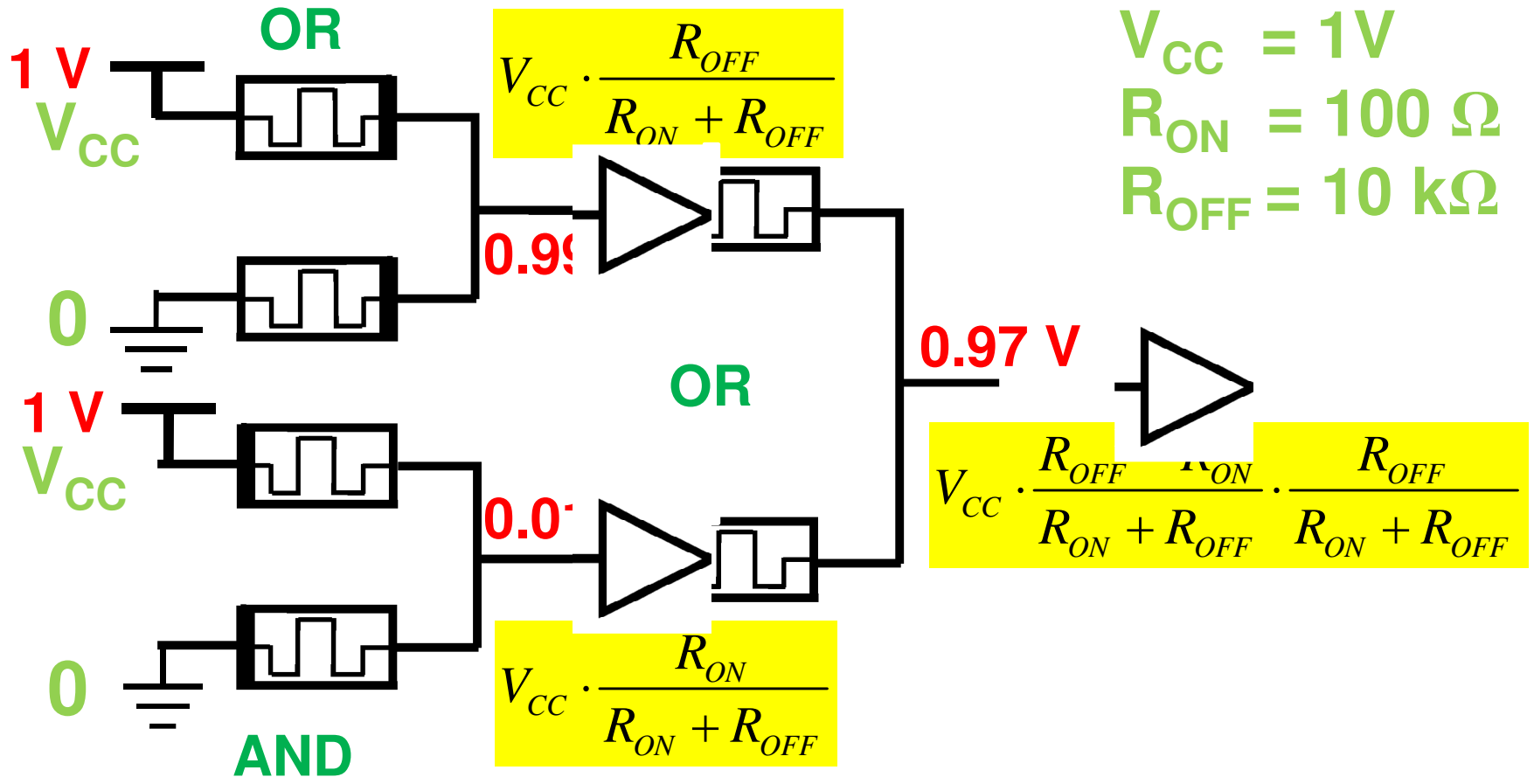
Decrease resistance



Increase resistance

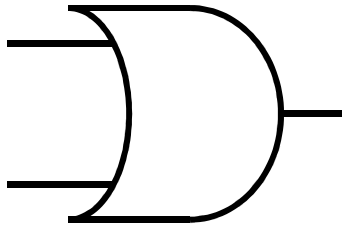
Need for Amplification

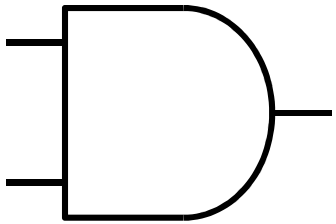
- Concatenation of memristor-based logic gates



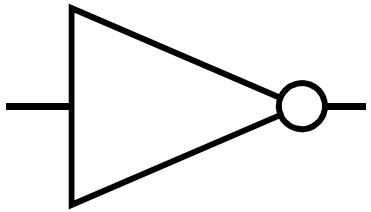
Need for Inversion

- AND and OR are not computationally complete



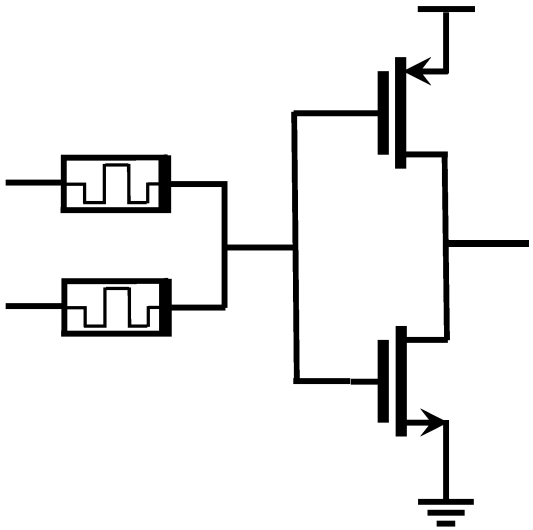


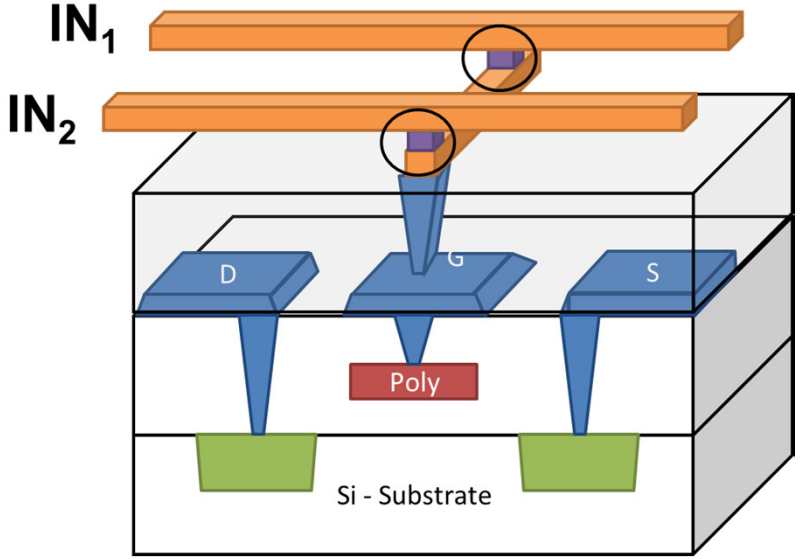
- Need for NOT



CMOS Compatibility

- Memristors can be fabricated with CMOS
- Input/output are voltages – as in standard CMOS logic
- Using CMOS inverter





J. Borghetti etl al, "A Hybrid Nanomemristor/Transistor Logic Circuit Capable of Self-Programming," PNAS 2008

Outline

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- **Eight bit full adder case study**
- Additional Issues
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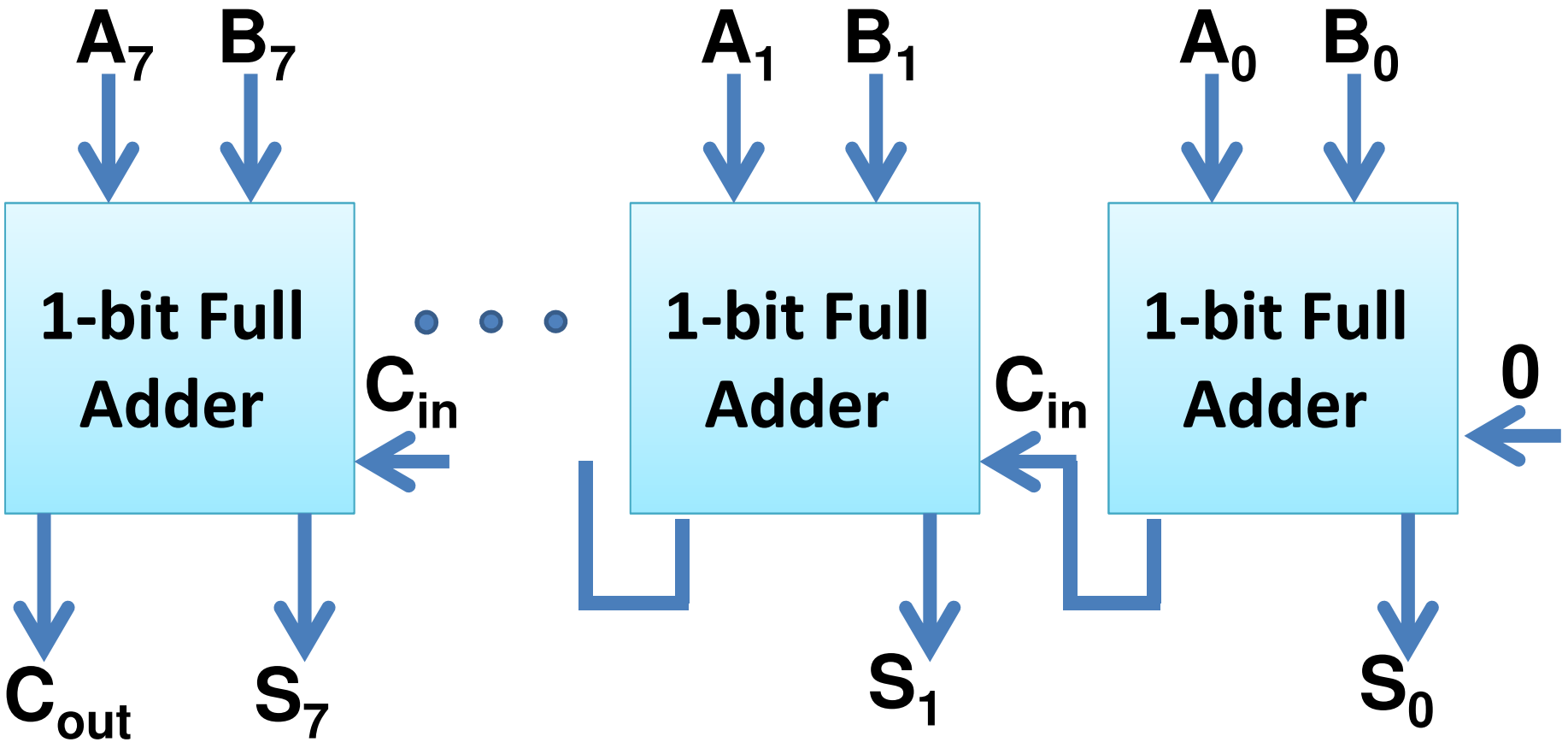
8-bit Full Adder Example

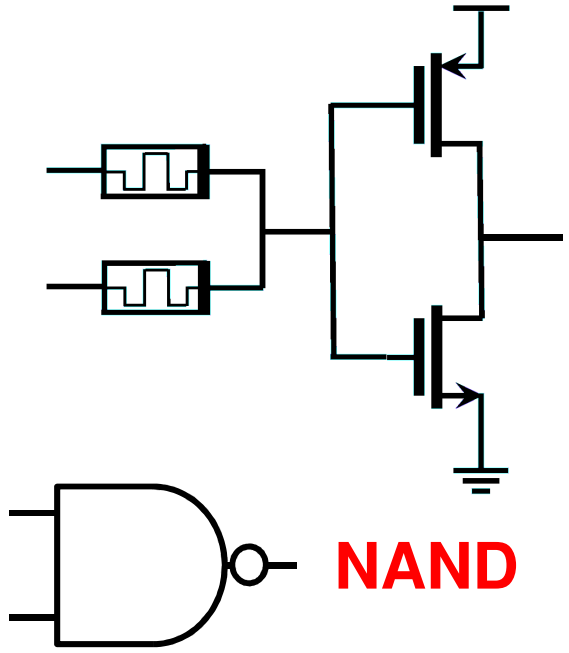


$$S_i = A_i \oplus B_i \oplus C_{i,in}$$

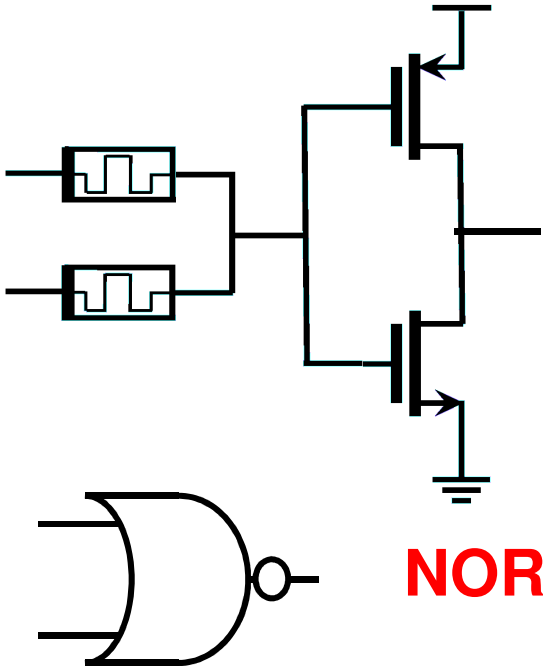
$$C_{i,out} = A_i \cdot B_i + C_{i,in} \cdot \left(A_i \oplus B_i \right)$$

Standard Cell Approach

- MRL standard cells – NAND and NOR
- Robust - no current leakage between stages
- Two CMOS-memristor cross-layer connections per cell – consume area and power



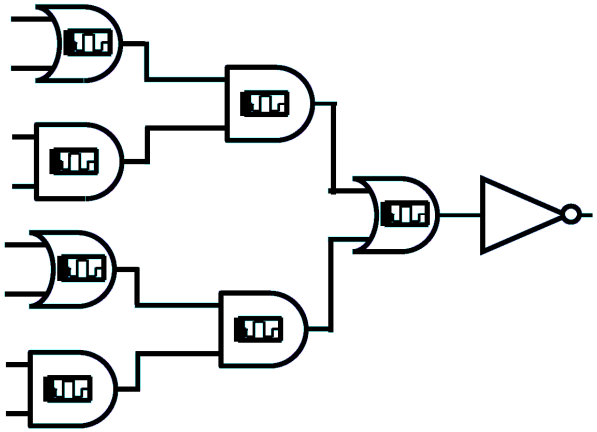
NAND



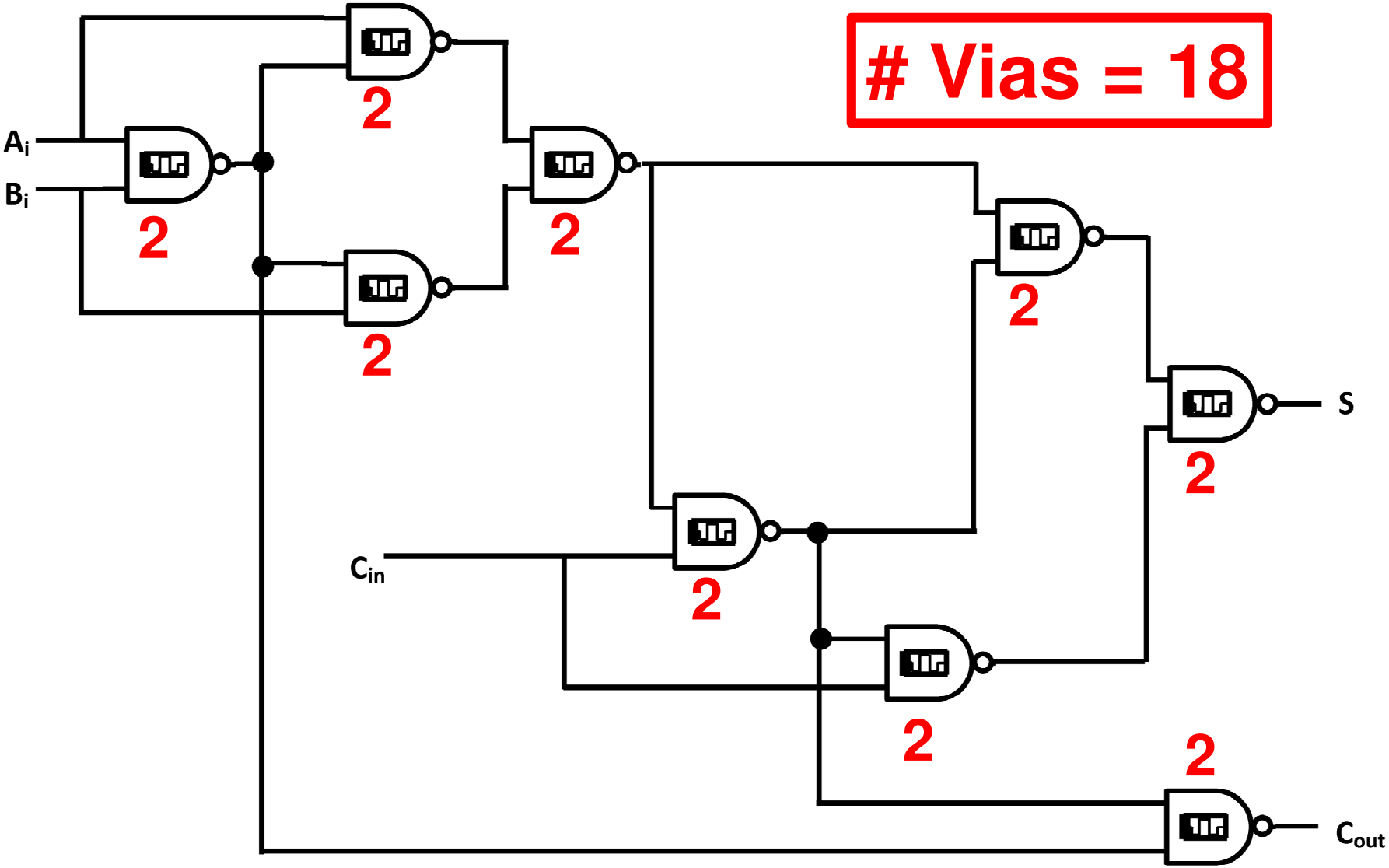
NOR

Optimized Approach

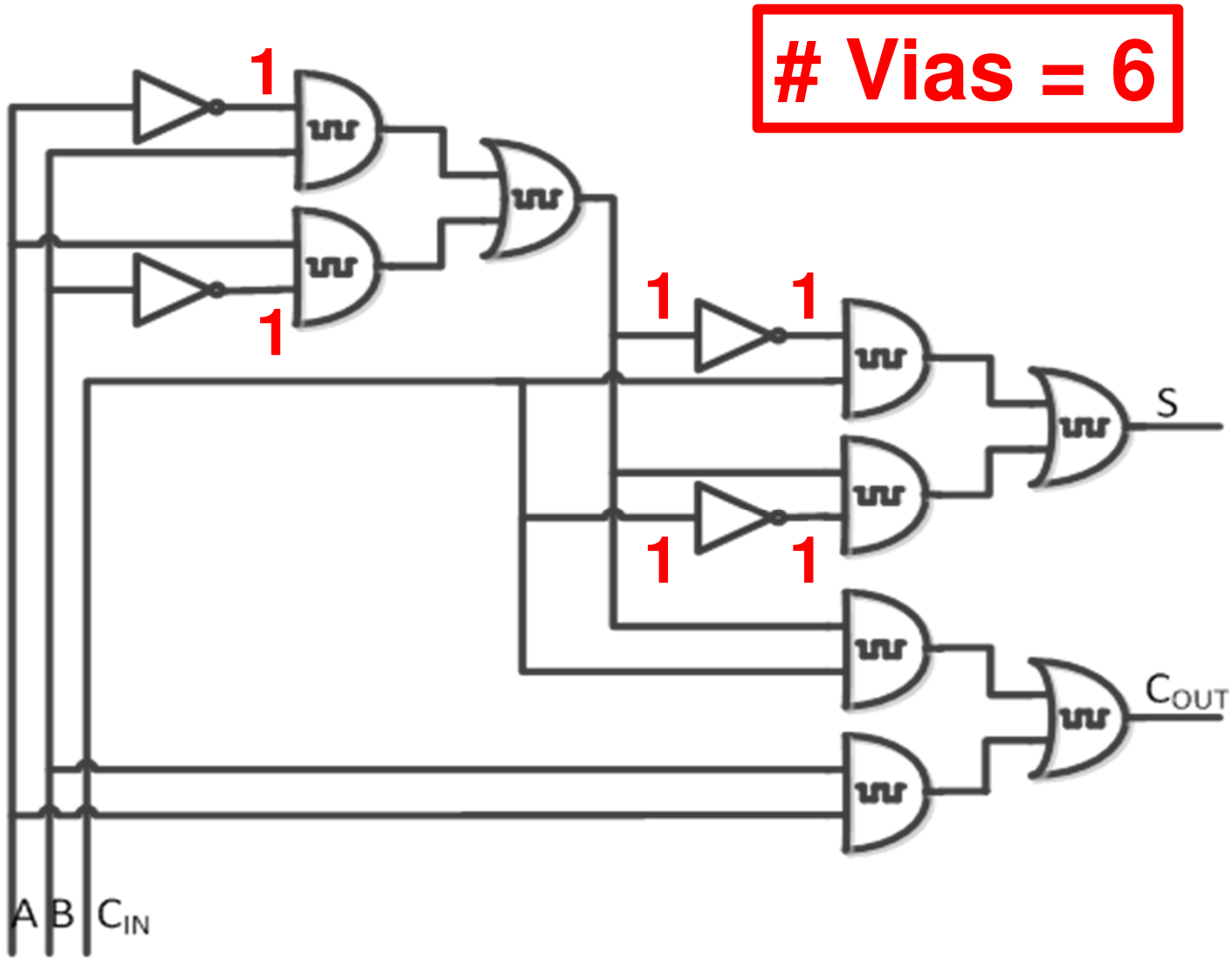
- **Target** - minimize CMOS-memristor cross-layer connections
- **Solution** – use inverters only when needed
  - Signal restoration (voltage optimization)
  - Logic function requires inversion



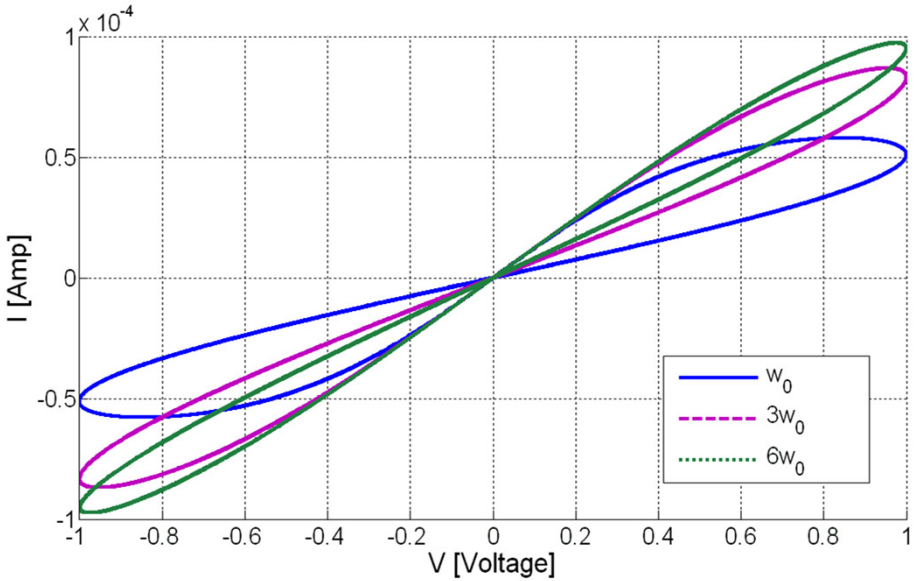
One Bit Standard Cell MRL Full Adder



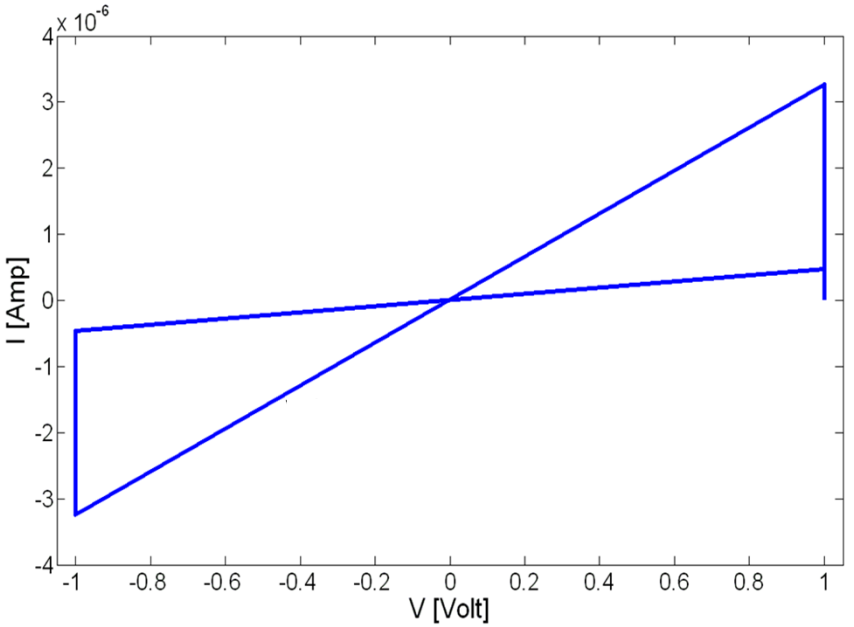
One Bit Optimized MRL Full Adder



Varying Degree of Nonlinearity



Linear memristor



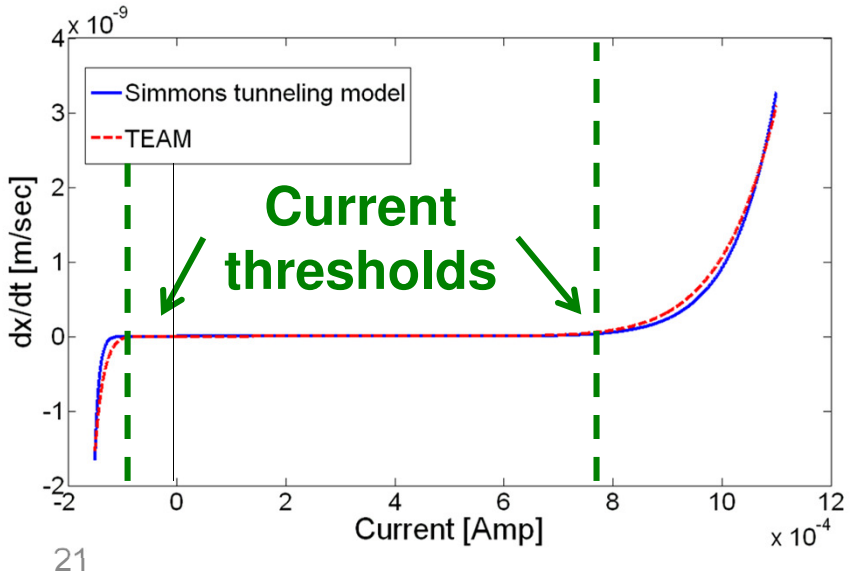
Highly nonlinear memristor

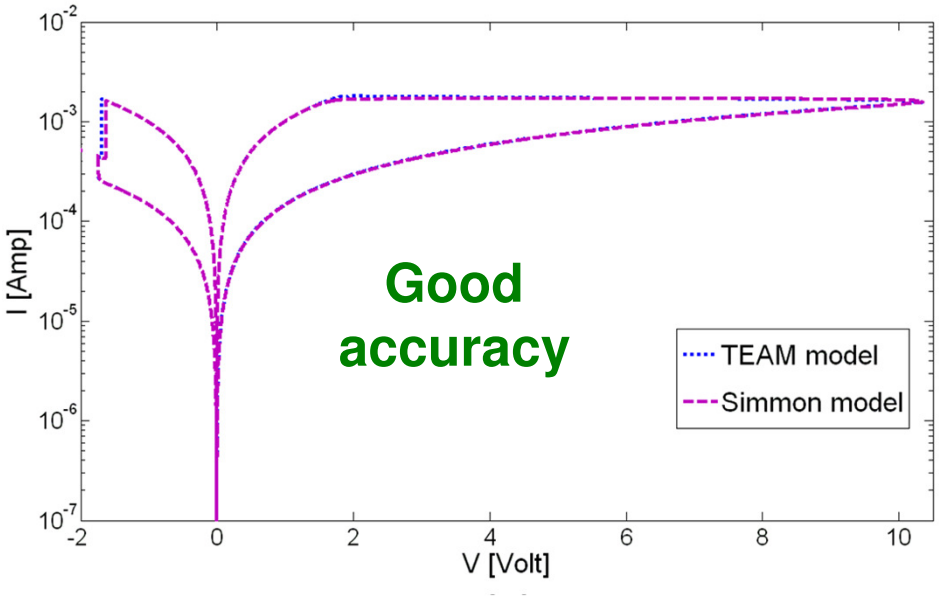
Testing Different Memristors
General Model – TEAM
ThrEshold Adaptive Memristor

- Tunable nonlinearity
- Current threshold

$$\frac{dx(t)}{dt} = \begin{cases} k_{off} \cdot \left(\frac{i(t)}{i_{off}} - 1 \right)^{\alpha_{off}} \cdot f_{off}(x), & 0 < i_{off} < i \\ 0, & i_{on} < i < i_{off} \\ k_{on} \cdot \left(\frac{i(t)}{i_{on}} - 1 \right)^{\alpha_{on}} \cdot f_{on}(x), & i < i_{on} < 0, \end{cases}$$

x – state variable





S. Kvatinsky et al, "TEAM: ThrEshold Adaptive Memristor Model," TCAS I, 2012

Case Study Results

- Linear memristors have better performance, area, and power in MRL
- Approx. 50% area reduction as compared to CMOS-based full adder

Parameter set	#memristors	# CMOS transistors	# vias	Power [norm.]
CMOS – based	-	288	-	-
Standard cell	144	144	144	1
Optimized (linear)	144	160	80	0.72
Optimized (nonlinear)	144	256	96	355

Outline

- Motivation / Why logic with memristors?
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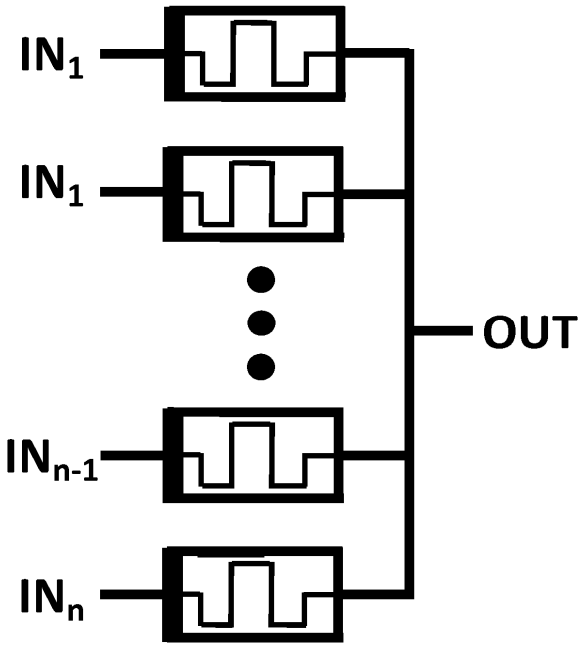
- **Additional Issues**
- Conclusions

Additional Issues
(In the Paper but Not in This Talk)

- Design considerations
  - Dynamic hazards
  - Power
- Multiple input MRL gates



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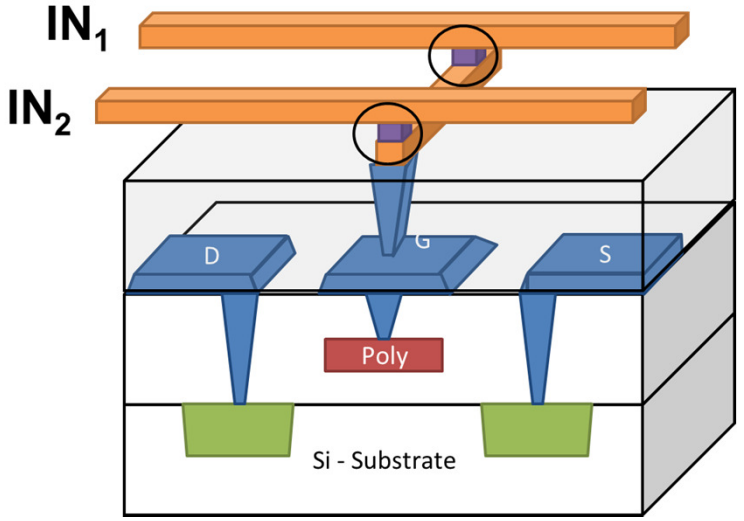
- **Conclusions**

MRL – Hybrid Memristor-CMOS Logic

- Approx. 2X improvement in logic density
- Memristor-based OR and AND
- Standard cell – NAND and NOR
- Optimized approach
- Linear memristor is better



Thanks!

http://memristor.shorturl.com