Logic Design with Unipolar Memristors

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***Abstract*—Memristors are novel devices that could naturally be designed as memory elements. Recently, several methods of designing memristors for logic operations have been proposed. These methods, mostly, make use of bipolar memristors. In this paper, we propose a method for performing logic with unipolar memristors based on OR and NOT logic gates. An integration of the basic building blocks into more complicated logic functions is described and demonstrated. Our results indicate that any logic function could be performed using an external controller. Thus, adding the capability of performing logic computations to numerous types of unipolar memristive materials in addition to their memory capability.**

Keywords— memristors; thin film; logic design; unipolar;

I. INTRODUCTION

As transistors continue shrinking, leakage current increases. In contemporary microprocessors, leakage has ceased being a negligible part of the power consumption. This fact is a key motivation for using non-volatile devices, such as memristors, in processing elements to reduce leakage current. Memristors are non-volatile circuit elements, predicted in 1971 by Leon Chua [1]. In 2008, Hewlett Packard laboratories were the first to link resistive switching materials to the theory of memristors [2]. As Chua suggested, we refer to all memristive devices as memristors [3], in the sense that all of the latter are two-terminal non-volatile memory devices based on resistance switching. Many types of materials can be associated with memristive behavior. These materials vary from molecular and ionic thin film semiconductors, through spin based and magnetic memristive systems, to phase change memories [4-6].

Switching in a memristive device, refers to the transition from one resistance state to another. Commonly, we distinguish between a high resistance state (HRS="OFF") and a low resistance state (LRS="ON"). In this paper, LRS and HRS are considered, respectively, as logical '1' and '0'. One prominent distinction of switching mechanisms is the classification of bipolar and unipolar switching. This classification is illustrated in Fig. 1. For bipolar switching, a transition from HRS→LRS (SET) occurs at a negative voltage, while the transition from LRS→HRS (RESET) occurs at a positive voltage. In the case of unipolar switching, a transition from HRS→LRS occurs when crossing a voltage threshold (V_{SET}), the current needs to be limited below a compliance current to avoid overloading the device. Resetting back to the OFF state happens at a voltage below V_{SET} and above V_{RESET}. A higher current is needed for switching to the OFF state. Unlike bipolar memristors, both transitions are independent of the voltage polarity.

The exact physical mechanism that promotes switching

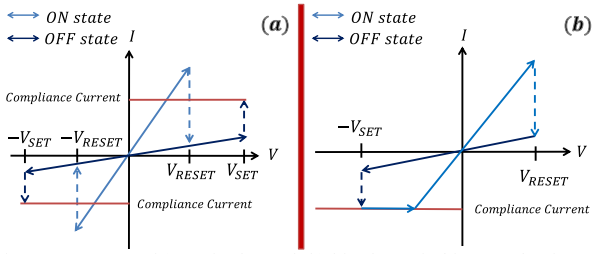

Fig. 1. I-V curve of (a) unipolar and (b) bipolar switching mechanisms of memristors.

differs between devices and can be generally classified as thermal, electronic, or ionic. Bipolar switching is linked to cation/anion migration whereas unipolar switching is linked to the creation or dissolution of conducting filaments – this is often referred to as the fuse-antifuse mechanism [7]. Both bipolar and unipolar memristors have already been incorporated into memory designs, and are also suggested to be used for performing logic operations [8-11]. Most of the proposed memristive logic families are appropriate solely to bipolar memristors.

Bipolar devices are attractive since the switching of the resistance occurs at lower voltage regimes as compared to unipolar [12]. Unipolar switching phenomenon, however, exists in numerous materials. Some unipolar resistive switching technologies, such as Phase Change Memory (PCM), have already been developed for commercial use and are more advanced and mature than bipolar memristive technologies. Additionally, a clear advantage of using unipolar switching devices for logic computation is the natural symmetry in polarity which allows easier incorporation in memory arrays whilst eliminating the concerns of current sneak paths and write disturbs using simple selector devices such as a diodes. Some unipolar memristors have high R_{OFF}/R_{ON} ratio (HRS/LRS ratio), which makes them attractive candidates to perform logic operations due to their high noise margin.

This paper focuses on logic with unipolar thin film devices. We propose a technique to perform OR and NOT logic gates with unipolar memristors that can easily be extended to execute any logical function. Our work has been tested in simulations using a modified Verilog-A model, based on [13] to fit TiO_2 thin film unipolar memristors. The proposed method could also be modified to suit other unipolar materials as well. Unlike previously proposed logical techniques for unipolar memristors [14-15], the proposed technique is based on intuitive building blocks (OR/NOT). Additionally, it could naturally be integrated

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into a memory since only resistance is used to represent logical values throughout the operation, just as data is stored within memristive memories. The proposed unipolar logic circuit can be easily modified to enable logic execution with Phase Change Materials (PCM) and may be suited for various types of unipolar memristive devices.

The rest of the paper is organized as follows. The basic concept of the proposed logic with unipolar memristors is described in section II. The building blocks of the proposed logic family (OR and NOT gates) are presented, respectively, in sections III and IV. Timing considerations for the logic gates are discussed in section V. The design of an advanced logic function is demonstrated in section VI, followed by evaluation of speed, area, and power, and a comparison to bipolar memristive logic in Section VII.

II. Logic with Unipolar Thin Film Memristors

The basic mechanism of the proposed logic technique is a voltage divider between two resistive elements - a memristor and a resistor for a NOT gate or two memristors for an OR gate. Connecting two resistive elements in series and applying a voltage bias; the ratio of voltages on the two elements complies with the ratio of their resistance, *i.e.*, the states are distinguished using a bias voltage. The first stage of operation is translating resistance to resistive states. The applied voltage for distinction is called the *preset voltage*.

After state distinction has been achieved, a higher voltage is applied to the circuit, adding higher applied voltage across both elements, regardless of their states. The voltage in this stage is predetermined to a value that promotes switching if necessary for proper execution, thus this voltage is called the *evaluation voltage*. The operation is therefore comprised of two execution stages – *preset* and *switching*.

One obstacle to operate properly arises from the fact that every change in resistance immediately changes the voltages, hence, possibly changing the distinction between states. This may lead to an incorrect result. Therefore maintaining the initial voltage distinction is required for a sufficient time to reach the desired resistance (HRS or LRS). One possible solution is to incorporate capacitors in the circuit in parallel with the memristors. Since capacitors take time to charge/discharge, they add delay to the system, thus we call them *suspension capacitors*. In addition to prolonging the validity of voltage values in the switching stage, suspension capacitors also delay the preset stage and in the case of the NOT gate, are actually mandatory for proper operation. Furthermore, the transition from preset to switching stages cannot be instantaneous. Hence, the intermediate evaluation stage is abstractly depicted as a transitive state and three stages are used to execute the operation as illustrated in Fig 2.

A. Preset Stage

In the preset stage, a voltage V_{PRESET} is applied to the circuit to charge the capacitors to initial voltage divider values. The applied voltage is high enough to distinguish between resistive states, but lower than the switching voltage. After sufficient time, approximately no current passes through the capacitors and their voltages are consistent with the voltage divider.

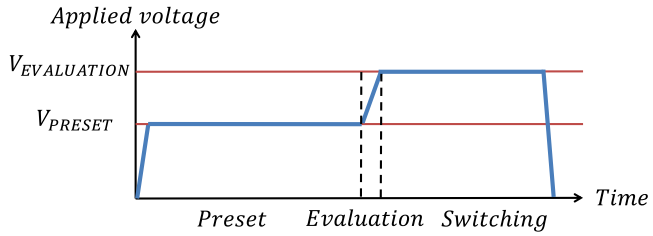

Fig. 2. The sequence of the applied voltage for the three stages of a general logic operation. The preset voltage distinguishes between logical states and charges the suspension capacitors. The evaluation stage converts the preceding voltages to the required voltages for switching.

B. Evaluation Stage

The evaluation stage starts immediately after the preset stage. A voltage pulse $V_{EVALUATION}$ is applied to the circuit. The purpose of this stage is to increase the voltage on both elements abruptly. The final voltage in this stage depends on the final voltage of the preset stage, hence correlates with the resistance of the circuit elements. However, the voltage increase $V_{EVALUATION} - V_{PRESET}$ is fixed for all scenarios. The exact increase in voltage after the voltage jump is determined by the capacitance ratio (charge sharing). Generally, branches with less capacitance gain more of the voltage increase.

C. Switching Stage

In the switching stage, $V_{EVALUATION}$ is still applied for sufficient time to allow switching of the memristors. The key is to choose proper pulse length and voltage magnitude to switch the memristors according to the desired logical functionality.

III. OR Gate

A two-input OR gate consists of two unipolar memristors U_1 and U_2 connected in series, with suspension capacitors connected in parallel to each memristor, as shown in Fig 3. The initial logical state of the memristors is the input of the gate and after execution both memristors have the same logical state, which serves as the output of the gate.

Assume $V_{SET} > V_{RESET}$, for proper behavior of the gate certain conditions need to be fulfilled. First, when both inputs are identical (*i.e.*, both are logical '1' or '0') there is no memristor switching. Second, when the inputs are different, the HRS memristor (in logical '0') has to switch to LRS since the desired output is logical '1'. Assuming that the voltage on the HRS memristor equals V_{PRESET} in the preset stage and $V_{PRESET} + \frac{1}{2}(V_{EVALUATION} - V_{PRESET})$ in the evaluation stage; the constraints on the voltages are therefore

$$V_{PRESET} < 2V_{RESET}, \quad (1a)$$

$$2V_{SET} - V_{PRESET} < V_{EVALUATION} < 2V_{RESET}. \quad (1b)$$

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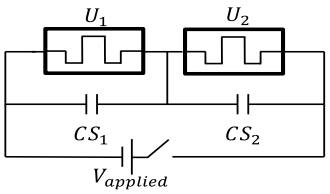

Fig. 3. Schematic of an OR gate. The input memristors U_1, U_2 are overwritten with the output (changed/unchanged memristive states).

Fig. 4 shows simulation results of an OR gate for the case where the inputs are different and U_2 switches for proper result. Note that when U_1 is logical '0' and U_2 is logical '1', the operation is destructive, *i.e.*, the value of the inputs is overwritten.

IV. NOT GATE

The NOT gate consists of a single unipolar memristor connected in series with a reference resistor. The memristor acts as both input and output of the NOT gate. For proper operation both the memristor and the resistor have a suspension capacitor connected to them in parallel as shown in Fig. 5. Without the suspension capacitors, $V_{EVALUATION}$ must be absurdly high for switching in the case of RESET operations. The resistance of the reference resistor is between LRS and HRS. This value ensures that the voltage at the end of the preset stage across a HRS (LRS) memristor is high (low), as illustrated in Fig. 6. A reasonable choice is $R_{REF} = \sqrt{R_{OFF}R_{ON}}$. For proper operation, the conditions on the applied voltage are

$$V_{PRESET} < min\left\{\sqrt{\frac{R_{OFF}}{R_{ON}}}V_{RESET}, V_{SET}\right\}, \quad (2a)$$

$$V_{EVALUATION} > \frac{1}{\gamma} max\left\{V_{SET}, V_{RESET} + V_{PRESET}\right\}, \quad (2b)$$

$$V_{EVALUATION} < \frac{1}{\gamma}(V_{SET} + V_{PRESET}), \quad (2c)$$

where $\gamma \triangleq \frac{C_{REF}}{C_{REF}+C_{S_1}}$.

V. TIMING CONSIDERATIONS

One of the critical points for proper behavior of the proposed logic technique is to apply the right voltage for a sufficient time during the switching stage. In this section, the timing constraints in the switching stage are explored. Assume τ_{SET} (τ_{RESET}) is a minimal transition time from HRS (LRS) to LRS (HRS) [15]. For successful switching, the duration of the switching stage must be greater than the minimal required switching time. The minimum condition on the length of the stage is therefore

$$T_{pulse} > max\{\tau_{set}, \tau_{reset}\} = T_{pulse,min}. \quad (3)$$

At the beginning of the switching stage, each memristor is biased with a voltage which promotes switching (if necessary). The validity of the specified voltage level is maintained for a short period of time, due to the use of suspension capacitors,

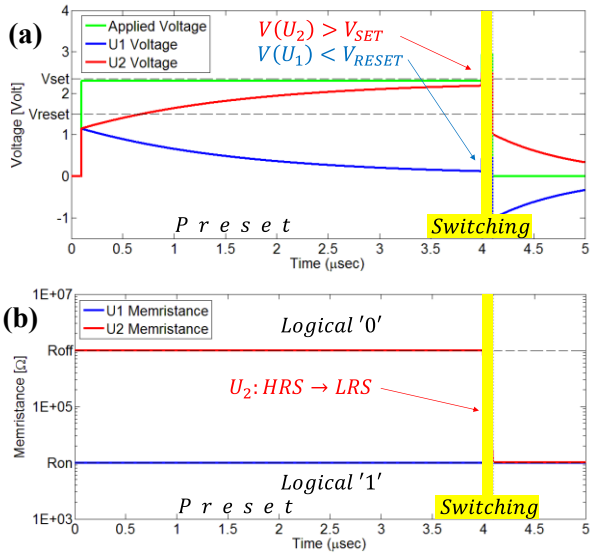

Fig. 4. OR gate simulation results. U_1 and U_2 are initialized to, respectively, LRS (logical '1') and HRS (logical '0'). (a) Voltages across the memristors during the operation, and (b) their resistance. In the first 4 μsec the system is in the preset stage, and the capacitors are charged/discharged to distinctive voltages. In the switching stage, U_2 voltage is higher than V_{set} for sufficient time and its logical value is switched to logical '1' as desired.

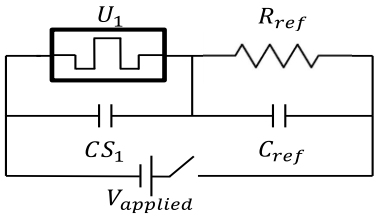

Fig. 5. Schematic of a NOT gate. A resistor is used as a reference to determine the state of the memristor.

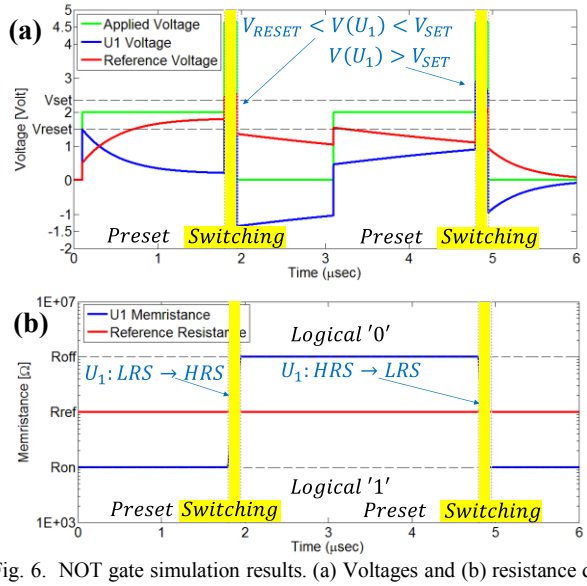

Fig. 6. NOT gate simulation results. (a) Voltages and (b) resistance during two consecutive memristor switching. In the first 3 μsec, U_1 switches from $LRS \rightarrow HRS$. In the second NOT operation U_1 switches back to LRS.

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but will eventually become invalid. If the switching stage is not terminated in time, a memristor might reach a voltage range which promotes the opposite transition, *i.e.*, reverse switching. The maximal length of the switching stage is determined according to the transient analysis of voltages in the circuit, and might be different for SET and RESET operations. For this purpose it is possible to define T_{SET} (T_{RESET}) as the approximate period of time in which the conditions for a SET (RESET) operation are met. It is important to understand that while τ_{set} and τ_{reset} are properties of the memristor, T_{SET} and T_{RESET} are determined by the selection of the different circuit parameters, namely $V_{PRESET}, V_{EVALUATION}, R_{REF}, C_{REF}, C_S$ and T_{PRESET}. Hence, the maximum condition on the length of the switching stage is

$$T_{pulse} < min\{T_{SET}, T_{RESET}\} = T_{pulse,max}. \quad (4)$$

To comply with both minimum and maximum conditions, both (3) and (4) must apply, as illustrated in Fig. 7. The parameters $V_{PRESET}, V_{EVALUATION}, R_{ref}$, and the switching capacitors can be chosen to support (3) and (4). Different circuit parameters, however, may lead to a reduction in performance. For example, larger capacitors ease the maximum condition, but slow the preset stage and increase power consumption.

VI. Advanced Logic Functions

OR and NOT functions form a complete logic structure. One major difference between the suggested logic gates and conventional CMOS logic is the destructive nature of the operations, *i.e.* the result of the operation overwrites the input. To resolve this issue a backup memristor with a copy of the initial value can be assigned through an OR operation with a memristor which is initialized to HRS.

To perform advanced logic operations, a function could be disassembled to its basic ingredients (OR, NOT). Each basic function of the computation should occur at a different time, and in a predetermined order. We show here a CMOS-based passgates design to select which logic operation (OR/NOT) to perform. Example of $NAND(U_1, U_2)$ operation is listed in Table I. The schematic of a NAND gate is shown in Fig. 8. Another option is to execute the advanced function in a manner similar to bipolar stateful logic within memory [10].

VII. Evaluation and Comparison

This section evaluates the proposed circuits in terms of speed, power, and area, and compares them to previously proposed memristive logic families that are suitable for bipolar memristors. In terms of speed, the need for a long preset stage is a disadvantage of the proposed mechanism. To accelerate the preset stage, higher voltages can be used in the cost of higher power consumption. Our simulations show that for a memristor with switching time τ, the delay time of a basic logic gate (OR\NOT) is approximately $10 \cdot \tau$.

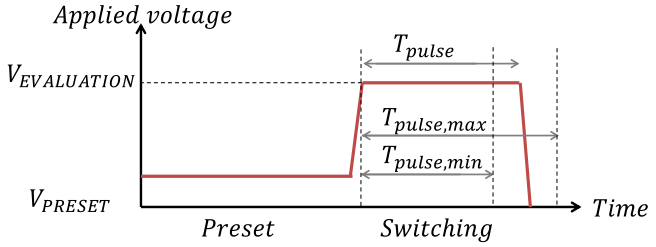

Fig. 7. Applied voltage duration in the switching stage. T_{pulse} satisfies (3) to reach the desired resistance and also meets (4) to avoid reverse switching.

TABLE I. NAND OPERATION USING A SEQUENCE OF OR AND NOT GATES

Stage	Operation	Logical	S_{OR}	S_{NOT}
1	NOT	$U_1 \leftarrow \overline{U_1}$	0	1
2	NOT	$U_2 \leftarrow \overline{U_2}$	0	1
3	OR	$U_1 \leftarrow \overline{U_1} + \overline{U_2}$, $U_2 \leftarrow \overline{U_1} + \overline{U_2}$	1	0

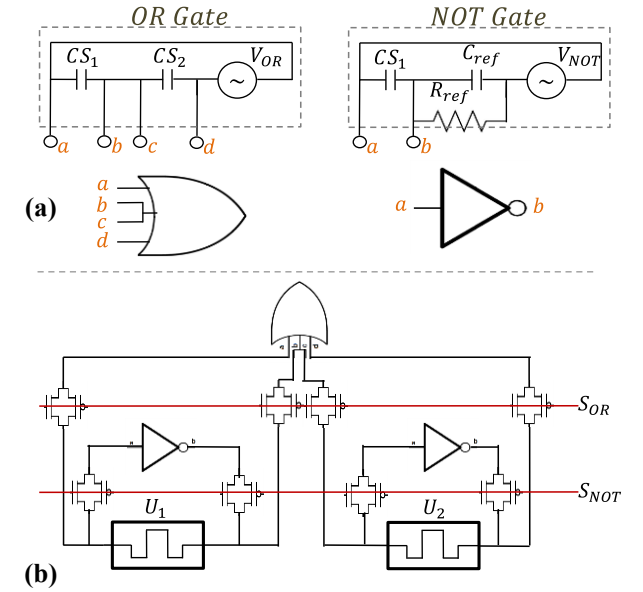

Fig. 8. (a) OR and NOT gate symbols and schematics and (b) schematic of a NAND gate based on the proposed OR and NOT gates. The signals S_{OR} and S_{NOT} control the sequence of operations through CMOS passgates.

In terms of area, the basic cell that would be incorporated into a crossbar array consists of a memristor and a capacitor. Suspension capacitors increase the area of the memory cell; the exact area depends on the switching time of the memristor. For example, memristors with switching time of 1ns require suspension capacitors with capacitance of approximately 0.8pF. The usage of suspension capacitors clearly impacts power consumption. Furthermore, the use of several computing phases (preset-switching) requires a clock that contributes to the power consumption and needs to be considered as well.

Some bipolar logic techniques for computation within memory are IMPLY [10] and MAGIC [11]. IMPLY and MAGIC are stateful logic techniques, similar in nature to the proposed technique. In both techniques, logical state is represented by resistance and the computation consists of multi-

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TABLE II. LATENCY AND AREA OF DIFFERENT FUNCTIONS USING OR, NOT AND COPY

Operation	# OR	# NOT	# COPY	# Backup	Latency
NOT	0	1	0	0	1
OR	1	0	0	0	1
NAND	1	2	0	0	3
NOR	1	1	0	0	2
AND	1	3	0	0	4
XOR	3	4	2	2	9
ADD 1 bit	4	7	2	2	13
Add N bit	11N-7	14N-7	9N-7	5	34N-21

TABLE III. LATENCY AND AREA OF *N*-BIT ADDER WITH DIFFERENT MEMRISTOR-BASED LOGIC METHODS, OPTIMIZED FOR MINIMUM AREA

Method of Execution	Latency (# Cycles)	Area (# Memristors)
IMPLY (Serial) [10]	29N	2
MAGIC [17]	15N	5
Unipolar Evaluation (This work)	34N-21	5

stage voltage application. Similarly to our proposed unipolar technique, in IMPLY the input data is overwritten with the output result. To compare the performance and area of the different techniques, we have evaluated a test case of an *N*-bit adder.

Assume the operation is incorporated in a crossbar that is optimized for area, *e.g.*, only a single operation can be performed at a clock cycle and backup devices can be discarded after usage. Table II lists the latency and number of backup memristors needed for different logical operations. A single bit addition can be performed in 13 cycles. An *N* bit addition can be performed in 34*N*-21 cycles. Table III compares this result with existing bipolar logic families. Note that due to the requirement of a long preset stage, the operated frequency of the proposed method is probably lower than the bipolar methods, thus possibly reducing the performance.

VIII. CONCLUSIONS

Combining data storage and processing is appealing since it can solve the critical issues in modern computing such as the limited memory bandwidth and power consumption. Both unipolar and bipolar memristors enable the execution of logic operations within memory using different methods. Since it is still unclear whether unipolar or bipolar mechanisms will become dominant for data storage, both phenomena are with interest. In this paper, we focus on unipolar mechanism and propose a logic technique for these device using OR and NOT gates.

The proposed technique can be naturally integrated within memristive crossbar memory. We have evaluated the proposed technique and compared it to bipolar logic techniques. The proposed technique can fit different unipolar technologies and we plan to further evaluate and investigate its implications on emerging technologies such as Phase Change Memory and 3D Xpoint, as well as exploring the opportunities for novel computer architectures.

IX. ACKNOLEDGMENTS

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REFERENCES

[1] L. O. Chua, "Memristor—The Missing Circuit Element," *IEEE Transactions on Circuit Theory,* Vol. 18, No. 5, pp. 507–519, September 1971.

[2] R. S. Williams, "How We Found the Missing Memristor", *IEEE Spectrum*, Vol. 45, No. 12, pp. 28-35, December 2008.

[3] L. O. Chua, "Resistance Switching Memories are Memristors," *Applied Physics A*, pp. 765 - 783, 2011.

[4] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM - ThrEshold Adaptive Memristor Model," *IEEE Transactions on Circuits and Systems I: Regular Paper,* Vol. 60, No. 1, pp. 211-221, January 2013.

[5] H.-S. P. Wong, *et al.*, "Phase Change Memory," *Proceedings of the IEEE,* Vol. 98, No. 12, pp. 2201 - 2227, December 2010.

[6] I. Y. Loh, "Mechanism and Assessment of Spin Transfer Torque (STT) Based memory", Ph.D. Dissertation, Massachusetts Institute of Technology, September 2009.

[7] R. Waser and M. Aono, "Nanoionics-Based Resistive Switching Memories," *Nature Materials,* Vol. 6, pp. 833 - 840, November 2007.

[8] Borghetti, J., Snider, G. S., Kuekes, P. J., Yang, J. J., Stewart, D. R., & Williams, R. S. (2010). 'Memristive'switches enable 'stateful'logic operations via material implication. *Nature*, 464(7290), 873-876.

[9] Kvatinsky, S., Wald, N., Satat, G., Kolodny, A., Weiser, U. C., & Friedman, E. G. (2012, August). MRL—memristor ratioed logic. In 2012 *13th International Workshop on Cellular Nanoscale Networks and their Applications* (pp. 1-6). IEEE.

[10] Kvatinsky, S., Satat, G., Wald, N., Friedman, E. G., Kolodny, A., & Weiser, U. C. (2014). Memristor-based material implication (IMPLY) logic: design principles and methodologies. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 22(10), 2054-2066.

[11] S. Kvatinsky et al., "MAGIC – Memristor Aided LoGIC," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 61, No. 11, pp. 895-899, November 2014.

[12] Yanagida, T., Nagashima, K., Oka, K., Kanai, M., Klamchuen, A., Park, B. H., & Kawai, T. (2013). Scaling effect on unipolar and bipolar resistive switching of metal oxides. *Scientific reports*, 3, 1657.

[13] Y. S. Kim and K.-S. Min, "Behavioral Current-Voltage Model with Intermediate States for Unipolar Resistive Memories," *Journal of Seminconductor Technology and Science*, Vol. 13, No. 6, pp. 539 - 545, December 2013.

[14] Sun, X., Li, G., Ding, L., Yang, N., & Zhang, W. (2011). Unipolar memristors enable "stateful" logic operations via material implication. *Applied Physics Letters*, 99(7), 072101.

[15] Cassinerio, M., Ciocchini, N., & Ielmini, D. (2013). Logic computation in phase change materials by threshold and memory switching. *Advanced Materials*,25(41), 5975-5980.

[16] W. Rainer, R. Dittmann, S. Georgi and K. Szot, "Redox-Based Resistive Switching Memories – Nanoionic Mechanisms, Prospects, and Challenges," *Advanced Materials*, Vol. 21, No. 25-26, pp. 2632 - 2663, July 2009.

[17] N. Talati, S. Gupta, P. Mane, and S. Kvatinsky, "Logic Design Within Memristive Memories Using Memristor-Aided loGIC (MAGIC)" *IEEE Transactions on Nanotechnology*, VOL. 15, NO. 4, PP. 635-650, JULY 2016.

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