VTEAM – A General Model for Voltage Controlled Memristors

Shahar Kvatinsky, *Member, IEEE,* Misbah Ramadan, Eby G. Friedman, *Fellow, IEEE,* and Avinoam Kolodny, *Senior Member, IEEE*

Abstract*— Memristors are novel electrical devices used for a variety of applications including memory, logic circuits, and neuromorphic systems. Memristive technologies are attractive due to the nonvolatility, scalability, and compatibility with CMOS. Numerous physical experiments have shown the existence of a threshold voltage in some physical memristors. Additionally, as shown in this paper, some applications require voltage controlled memristors to operate properly. In this paper, the Voltage ThrEshold Adaptive Memristor (VTEAM) model is proposed to describe the behavior of voltage controlled memristors. The VTEAM model extends the previously proposed TEAM model, which describes current-controlled memristors. The VTEAM model has similar advantages to the TEAM model: it is simple, general, and flexible and can characterize different voltage controlled memristors. The VTEAM model is accurate (below 1.5% in terms of relative root mean squared error) and computationally efficient as compared to existing memristor models and experimental results describing different memristive technologies.

Index Terms—**Memristive systems, memristor, SPICE, MATLAB, resistive switching, ReRAM.**

I. INTRODUCTION

Memristors are passive two-port elements with a variable resistance. For ideal memristors, as originally suggested by Chua in 1971 [1], the resistance depends directly on the charge passing through the device, or alternatively, on the integral over time of the applied voltage across the device (*i.e.*, flux). Memristive devices, originally defined by Chua and Kang [2], are an extension of the memristor definition, where the resistance depends on a state variable (or a set of state variables). While discussions exist in the literature concerning the specific definition of memristors [3], [4], [5], in this paper the term 'memristor' is used to describe both ideal memristors and memristive devices. Emerging nonvolatile memory technologies (*e.g.*, Resistive RAM, Phase-Change Memory, and Spin-Transfer Torque Magnetoresistance RAM) are considered as memristors [4]. Memristors can also be used for other attractive applications, such as logic circuits [24] and neuromorphic systems.

Numerous memristor models have been proposed. Some of the models do not exhibit a threshold [6], [7], [8]; hence, the resistance of the device changes for any applied voltage (or current). Recently, the TEAM model [9] has become widely used due to the simplicity, generality, accuracy, and low computational complexity. The TEAM model relies on a threshold current, where the resistance changes only for currents above a certain level. Experimental data of some memristive devices show, however, the existence of a threshold voltage rather than threshold current. Furthermore, certain memory and logic applications require memristors with a threshold voltage to operate properly.

Hence, a memristor model with the advantages of the TEAM model (*i.e.*, general, simple, and sufficiently accurate) and exhibiting a threshold voltage is desirable. In this paper, VTEAM, a novel memristor model that satisfies these requirements, is presented. The VTEAM model has sufficient accuracy (below 1.5% in terms of relative root mean squared error) as compared to existing memristor models and experimental results of different memristive technologies.

The rest of the paper is organized as follows. Motivation for a threshold voltage and applicability to various circuits are demonstrated in Section II. In Section III, the VTEAM model is described. A comparison between the VTEAM model and previously proposed models, including experimental results, is presented in Section IV. The paper is summarized in Section V.

II. MOTIVATION FOR THRESHOLD VOLTAGE

The authors previously proposed the TEAM model [9], which is inspired by the Simmons tunnel barrier model [8]. The TEAM model is based on a threshold current. The resistance of the memristor does not change for currents below a certain threshold current. Experiments on several types of memristive devices, however, have shown the existence of a threshold voltage (*e.g.*, [6], [18], [23]), as illustrated in Figure 1 for different memristors. Furthermore, a memristor with a threshold voltage is more appropriate than a threshold current for certain logic and memory applications, as demonstrated in subsections IIA and IIB for, respectively, memory and logic.

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S. Kvatinsky is with the Department of Computer Science, Stanford University, Stanford, CA 94305, USA. (Corresponding author e-mail: shahark@stanfod.edu).

M. Ramadan, and A. Kolodny are with the Department of Electrical Engineering, Technion – Israel Institute of Technology, Haifa 32000, Israel.

E. G. Friedman is with the Department of Electrical Engineering and Computer Engineering, University of Rochester, Rochester, NY 14627, USA.

A. *Motivation for Threshold Voltage for Memory*

A memristive crossbar is a common memristive memory structure [10]. In a crossbar, as shown in Figure 2, a write operation is performed by applying a voltage V_{set} or V_{rst} on a selected cell within the crossbar array to write, respectively, a logical one (*i.e.*, low resistance R_{ON}) and logical zero (*i.e.*, high resistance R_{OFF}). To write a logical zero to a memristor with a threshold current I_{th}, the current of the memristor $I(t)$ must be above the threshold current, namely,

$$I(t) = \left|\frac{V_{rst}}{R(t)}\right| > |I_{th}|, \quad (1)$$

where $R(t)$ is the resistance of the memristor. During the write operation, $R(t)$ increases and the current passing through the cell $I(t)$ decreases. The smaller current slows the writing speed. Additionally, for an insufficient write voltage V_{rst}, both performance and reliability issues can occur if (1) is not satisfied. To avoid these issues, higher currents are required, increasing the applied voltage V_{rst}.

High voltages, however, increase power and may lead to a destructive write operation in neighboring cells. For example, in Figure 2b, when $|V_{rst}| > |3 \cdot I_{th} \cdot R_{ON}|$ and $R^{(1)} = R^{(2)} = R^{(3)} = R_{ON}$, $|I_{SP}| = |V_{rst}|/(3R_{ON}) > |I_{th}|$ and the resistances $R^{(1)}$ and $R^{(3)}$ switch to R_{OFF}, creating an undesired partial OFF switching event in some of the neighboring memristors. For memristors with a threshold voltage, however, no performance and reliability issues exist since the applied voltage across each memristor is fixed and the OFF switching procedure is not affected by the variable resistance, as illustrated in Figure 2c.

B. *Motivation for Threshold Voltage in Logic Applications*

Another example of a memristive circuit that requires a threshold voltage is the MAGIC NOR gate [11]. A schematic of the MAGIC NOR gate is shown in Figure 3. In the MAGIC NOR gate, the inputs of the logic gate are the initial resistance of the input memristors (*i.e.*, memristors IN1 and IN2 in Figure 3), while the output memristor (*i.e.*, memristor OUT in Figure 3) is initialized to logical one (resistance of R_{ON}). Execution of the MAGIC NOR gate is achieved by applying a fixed voltage V_0 to the input memristors. The output of the MAGIC NOR gate is the logical state of the output memristor after execution, which depends upon the current passing through the device or, alternatively, the voltage across the device. The current passing through the output memristor depends on the total resistance of the circuit, and consists of the sum of the resistance of the two input memristors connected in parallel, and the output memristor.

For correct logical behavior, the resistance of the output memristor does not change when both inputs are logical zero (*i.e.*, the resistance of the circuit is $1.5R_{OFF}$), and changes for any other input set (as shown in Figure 3(c)). Specifically, when one input of the gate is logical zero (resistance of R_{OFF}) and the other input is logical one (R_{ON}, where $R_{OFF} \gg R_{ON}$), the resistance of the output memristor changes when switching from R_{ON} to R_{OFF}. Assume a memristor with current thresholds of $|i_{ON}| = i_{OFF} = 20\ \mu A$, and circuit parameters of $R_{ON} = 1\ k\Omega$, $R_{OFF} = 100\ k\Omega$, and $V_0 = 1\ V$. The current passing through the output memristor is

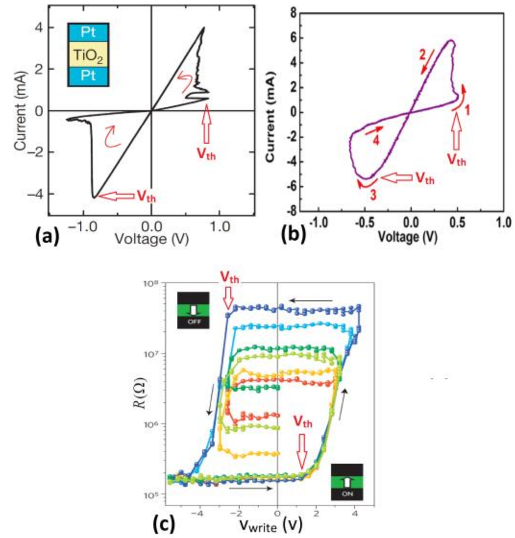


Figure 1. Current-voltage characteristics of memristors exhibiting a threshold voltage. (a) Pt-TiO$_2$-Pt memristor [6], (b) Ag/a-LSMO/Pt memristor [23], and (c) ferroelectric memristor [18].

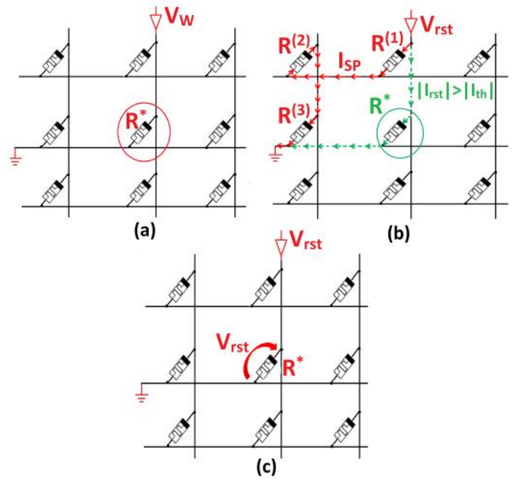


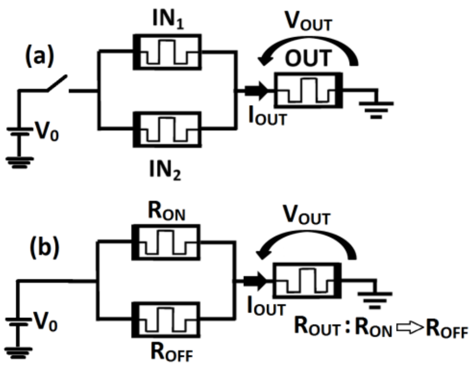
Figure 2. Illustration of a 3 x 3 memristive crossbar. (a) General write procedure. When the applied voltage V_S is V_{rst} or V_{set}, the resistance R^* switches, respectively, to R_{OFF} or R_{ON}. (b) Crossbar with memristors with threshold current. Applying a constant voltage V_{rst} switches R^* to R_{OFF}. The magnitude of the current I_{rst} decreases when the resistance R^* increases, delaying the transition. Additionally, increasing V_{rst} may cause a partial OFF switching event in the sneak path resistances. (c) Crossbar with memristors with threshold voltage. The applied voltage $|V_{rst}| > |V_{th}|$ is constant across R^* during switching to R_{OFF}.

$$I_{OUT}(t) = \frac{V_0}{(R_{ON} \parallel R_{OFF}) + R_{OUT}(t)} \approx \frac{V_0}{R_{ON} + R_{OUT}(t)} \geq I_{th}, \quad (2)$$

where $R_{OUT}(t)$ is the resistance of the output memristor, which increases from the initial value of R_{ON}. The current is reduced until a current threshold is exceeded and remains constant, as illustrated in Figure 3b. For this numerical example, $R_{OUT} = 49\ k\Omega < R_{OFF}/2$, which is considered logical one, producing an incorrect output.

For a memristor with a threshold voltage, however, full switching to R_{OFF} is achieved. V_{OUT}, the voltage at the output memristor, as shown in Figure 3, is

$$V_{OUT}(t) = V_0 \cdot \frac{R_{OUT}(t)}{R_{OUT}(t) + (R_{ON} \parallel R_{OFF})} \approx V_0 \cdot \frac{R_{OUT}(t)}{R_{OUT}(t) + R_{ON}}. \quad (3)$$



Input Set [#]	IN1	IN2	OUT
1	0	0	1
2	0	1	0
3	1	0	0
4	1	1	0

Figure 3. Schematic of MAGIC NOR gate. (a) Two input memristors IN_1 and IN_2, and output memristor OUT. The logical operation is achieved by applying a voltage V_0, and (b) MAGIC NOR gate illustrating the operation with inputs of IN_1='1' and IN_2='0'. (c) NOR truth table.

For proper operation (*i.e.*, switching to logical zero), the applied voltage V_0 must exceed the threshold voltage during the entire operation. From (3), V_{OUT} increases as R_{OUT} increases, hence a complete switch to R_{OFF} is achieved for memristors with a threshold voltage.

III. VOLTAGE THRESHOLD ADAPTIVE MEMRISTOR (VTEAM)

The VTEAM model is described in this section. Similar to the predecessor model (the TEAM model [9]), the VTEAM model is based on an expression of the derivative of the internal state variable. The VTEAM model combines the advantages of the TEAM model (*i.e.*, simple, general, accurate, and designer friendly) with a threshold voltage rather than a threshold current. The current-voltage relationship of the VTEAM model is undefined and can be freely chosen from any current-voltage characteristics. Several examples of possible current-voltage relationships are described in this section. Generally, a voltage-controlled time-invariant memristive device [2] is represented by

$$\frac{dw}{dt} = f(w,v), \tag{4}$$

$$i(t) = G(w,v)\cdot v(t), \tag{5}$$

where w is an internal state variable, $v(t)$ is the voltage across the memristive device, $i(t)$ is the current passing through the memristive device, $G(w,v)$ is the device conductance, and t is time. Note that $f(w,v)$ is a general function of the derivative of the state variable w. Specifically, these expressions allow the existence of a threshold voltage.

Analogous to the derivative of the state variable in the TEAM model, the derivative of the state variable in the VTEAM model is

$$\frac{dw(t)}{dt} = \begin{cases} k_{off}\cdot\left(\dfrac{v(t)}{v_{off}}-1\right)^{\alpha_{off}}\cdot f_{off}(w)\,, & 0<v_{off}<v \quad (6a)\\ 0\,, & v_{on}<v<v_{off} \quad (6b)\\ k_{on}\cdot\left(\dfrac{v(t)}{v_{on}}-1\right)^{\alpha_{on}}\cdot f_{on}(w)\,, & v<v_{on}<0 \quad (6c)\end{cases}$$

where k_{off}, k_{on}, α_{off}, and α_{on} are constants, and v_{on} and v_{off} are threshold voltages. The parameter k_{off} is a positive number, while k_{on} is a negative number. The functions $f_{off}(w)$ and $f_{on}(w)$ represent the dependence of the derivative of the state variable on the state variable w. These functions behave as window functions, which constrain the state variable to bounds of $w \in [w_{on}, w_{off}]$. Nevertheless, different window functions can be used, for example, the window functions [12], [13], [14], and [9], or perhaps an ideal rectangular window function where the derivative of w is zero when $w \notin (w_{on}, w_{off})$.

The current-voltage relationship is not inherently defined in the VTEAM model. A linear dependence of the resistance and state variable can be achieved, where the current-voltage relationship is

$$i(t) = \left[R_{ON} + \frac{R_{OFF}-R_{ON}}{w_{off}-w_{on}}\cdot(w-w_{on})\right]^{-1}\cdot v(t)\,, \tag{7}$$

where w_{on} and w_{off} are the bounds of the internal state variable w, and R_{ON} and R_{OFF} are the corresponding resistances of the device when the state variable is, respectively, w_{on} and w_{off}. Alternatively, an exponential dependence on the state variable can be assumed as in [8]. In this case, the current-voltage relationship is

$$i(t) = \frac{e^{-\frac{\lambda}{w_{off}-w_{on}}\cdot(w-w_{on})}}{R_{ON}}\cdot v(t)\,, \tag{8}$$

where λ is a fitting parameter, $e^{\lambda} = \frac{R_{OFF}}{R_{ON}}$.

IV. FITTING THE VTEAM TO OTHER MEMRISTOR MODELS AND EXPERIMENTAL DATA

The VTEAM model is a general model which can be fit to numerous memristor models and experimental data due to the inherent generality and robustness. Given the current-voltage characteristics of a specific memristor, a set of parameters is chosen to fit the VTEAM model to a reference I-V relationship. To fit the I-V curve, the relative root mean squared error is minimized using Gradient Descent [15] and simulated annealing algorithms [16]. The relative root mean square (RMS) error is

$$e_{i,v} = \sqrt{\frac{1}{N}\cdot\left(\frac{\sum_{i=1}^{N}\left(V_{VTEAM,i}-V_{ref,i}\right)^2}{\bar{V}_{ref}^2}+\frac{\sum_{i=1}^{N}\left(I_{VTEAM,i}-I_{ref,i}\right)^2}{\bar{I}_{ref}^2}\right)}\,, \tag{9}$$

where N is the number of samples, $V_{VTEAM,i}$ and $I_{VTEAM,i}$ are, respectively, the corresponding i-th sample of the voltage and current of the VTEAM model, $V_{ref,i}$ and $I_{ref,i}$ are, respectively, the corresponding i-th sample of the voltage and current of the reference model, and $\bar{V}_{ref}$ and $\bar{I}_{ref}$ are, respectively, the Euclidean norm of the voltage and current of the reference model.

The fitting procedure is iterated on k_{off} and k_{on} to minimize the error function given in (9). To avoid convergence to a local minimum rather than the optimal global fitting, the remaining fitting parameters (i.e., α_{off}, α_{on}, v_{off}, v_{on}, R_{OFF}, and R_{ON}) are manually chosen to exhibit a similarity (below 1.5% relative RMS error) to the reference I-V relationship. Furthermore, an ideal window function is used for the VTEAM model during the fitting procedure to bound the state variable, and the current-voltage relationship is chosen to be the original I-V relationship of the reference model. Fitting the VTEAM model to experimental data is presented in subsection A, following by fitting and a comparison to other memristor models in subsection B.

A. VTEAM Model vs. Experimental Data

In this section, three physical memristive devices are compared to the VTEAM model: a Pt-Hf-Ti memristor where the active switching layer has been prepared in the same manner as reported in [17], a ferroelectric memristor [18], and a single component metallic nanowire memristor [19]. The resulting parameters are listed in Table I, and the graphical results of the I-V relationship are depicted in Figure 4.

B. VTEAM Model vs. Previously Proposed Models

Previously proposed memristor models, such as the Yakopcic [20] and BCM [21] models, also exhibit a threshold voltage. Both models, however, operate according to a different state variable mechanism than the VTEAM model. The VTEAM model increases the resistance while moving the state variable w towards the boundary w_{off}. In the Yakopcic and BCM models, however, increasing the state variable decreases the resistance of the device. Although this difference is only based on a different definition and terminology, to accurately compare these models to the VTEAM model, a modification of the original models is required. The I-V relationship of both models is mirrored according to the V-plane and I-plane, *i.e.*, the opposite polarity of the voltage and current are used or, alternatively in circuit terms, the memristor is connected to the opposite polarity. The fit of the VTEAM model to the Yakopcic, BCM, and TEAM models is listed in Table II. In Figure 5, a graphical description of the I-V relationship is shown.

V. CONCLUSIONS

A memristor model that exhibits a threshold voltage is required to accurately characterize physical behavior and to apply to several memory and logic circuits. In this paper, the VTEAM model is presented, a model that exhibits a threshold voltage. The proposed model has the advantages of the TEAM model (*i.e.*, flexibility, generality, and sufficiently accurate).

A comparison between the VTEAM model to experimental data is provided. Sufficient accuracy of the VTEAM model to experimental data is achieved by tuning the fitting parameters, demonstrating generality and flexibility. The VTEAM model also exhibits sufficient accuracy while fitting to previously proposed memristor models with a threshold voltage. These models lack the generality of the VTEAM model and cannot be fit to experimental data.

The VTEAM and TEAM models exhibit, respectively, a threshold voltage and current. Together, these models are applicable to a variety of memristive technologies. These models have been implemented in Verilog-A for SPICE simulations [22], and can be used to design memristive circuits.

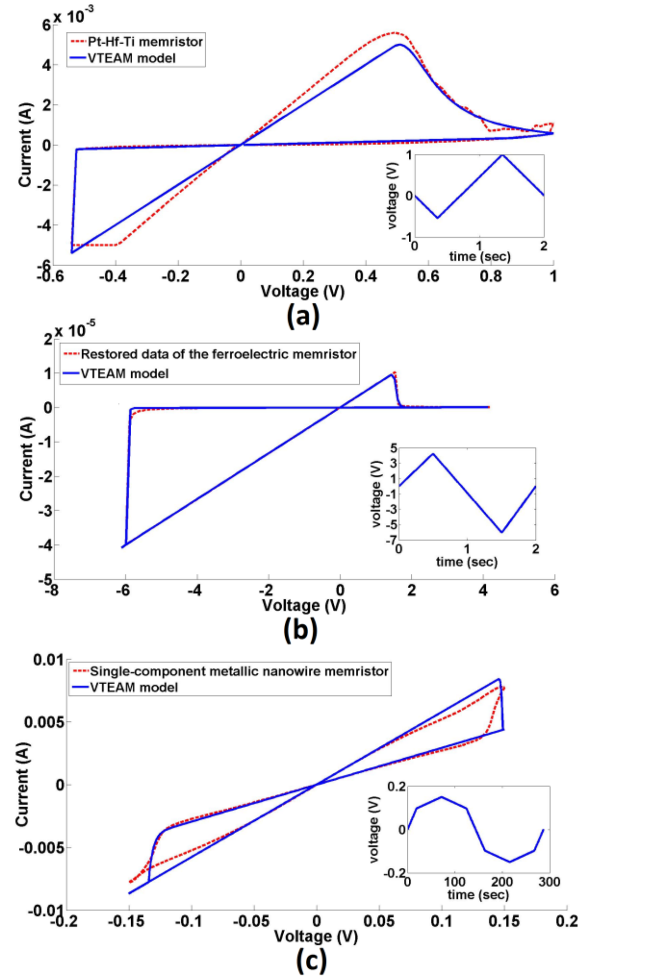


Figure 4. VTEAM model fit to experimental results. The VTEAM model is fitted to (a) a Pt-Hf-Ti memristor [17], (b) a ferroelectric memristor [18], and (c) a single-component metallic nanowire memristor [19]. The applied voltage across the devices are shown in the sub-window.

TABLE I. FITTING CHARACTERISTICS OF THE VTEAM MODEL TO EXPERIMENTAL MEMRISTIVE DEVICES.

Physical device		Pt-Hf-Ti memristor [17]	Ferroelectric memristor [18]	Metallic nanowire memristor [19]
Optimized parameters of the VTEAM model	α_{off}	1	5	3
	α_{on}	3	5	9
	v_{off} [v]	0.5	1.4	0.145
	v_{on} [v]	-0.53	-5.7	-0.09
	R_{OFF} [Ω]	$2.5 \cdot 10^{3}$	$5 \cdot 10^{7}$	34
	R_{ON} [Ω]	100	$1.5 \cdot 10^{5}$	17.3
	k_{off} [m/s]	$4.03 \cdot 10^{-8}$	10^{-4}	$5 \cdot 10^{-4}$
	k_{on} [m/s]	-80	-30	$-1.32 \cdot 10^{-6}$
	w_{off} [nm]	10	10	10
	w_{on} [nm]	0	0	0
	w_{init} [nm]	10	0	0
	i-v	linear	linear	exponent
$e_{v,i}$ minimal value achieved		1.12%	1.48%	0.41%

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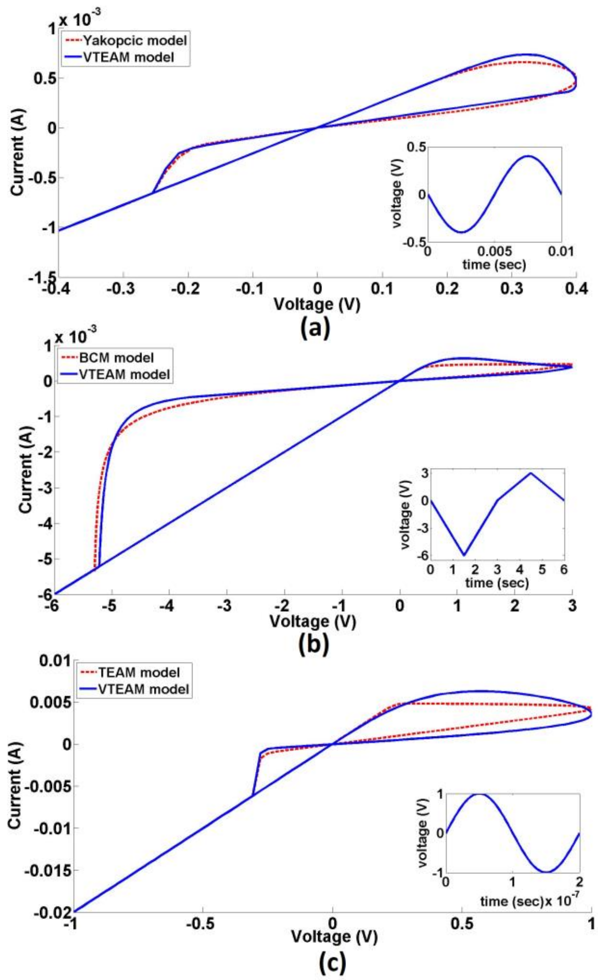

Figure 5. Comparison of VTEAM model to previously proposed memristor models. (a) Yakopcic model [20], (b) BCM model [21], and (c) TEAM model [9].

TABLE II. FITTING CHARACTERISTICS OF THE VTEAM MODEL TO OTHER MEMRISTOR MODELS.

Memristor model		Yakopcic [20]	BCM [21]	TEAM [9]
Optimized parameters of the VTEAM model	α_{off}	3	1	1
	α_{on}	3	1	3
	v_{off} [v]	0.16	0.15	0.02
	v_{on} [v]	-0.15	-3.5	-0.2
	R_{OFF} [Ω]	1069.5	10^4	10^3
	R_{ON} [Ω]	387	10^3	50
	k_{off} [m/s]	$2.49\cdot10^{-6}$	$5.46\cdot10^{-10}$	$5\cdot10^{-4}$
	k_{on} [m/s]	$-2.2\cdot10^{-4}$	$-7.34\cdot10^{-8}$	-10
	w_{off} [nm]	10	10	3
	w_{on} [nm]	0	0	0
	w_{init}[nm]	8.9	7.7778	0
	i-v relationship	linear	linear	linear
$e_{v,i}$ minimal value achieved		0.43%	0.09%	0.44%

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