Resume – Rotem Ben Hur

Personal Details

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Viterbi Faculty of Electrical Engineering
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Education and Qualification

2015- **M.Sc in Electrical Engineering,** Technion - Israel Institute of Technology, Haifa, Israel.
Advisor: Shahar Kvatinsky

2010-2014 **B.Sc in Electrical Engineering,** Technion - Israel Institute of Technology, Haifa, Israel.

2008 **Officers School,** IAF, IDF

2005 **Tae-Kwon-Do Instructor Training,** Wingate Institute, Israel

2004-2006 **Mae Boyer High School,** Jerusalem, Israel

Experience

2016- **Teaching assistant in "Logic Design",** Technion, Haifa

2016- **Supervisor of B.Sc projects**, Technion, Haifa

2014 **Teaching assistant in "Digital Systems",** Technion, Haifa

2012-2015 **Hardware Engineering Student,** Elbit Systems Ltd, Haifa
Research and development in the subject of programmable graphic cards for aircraft avionic systems. Main field of responsibility - logic design in VHDL environment.

2011-2012 **Instructor, "Noar Shocher Mada",** Technion, Haifa
Teaching gifted children various scientific subjects with emphasis on physics.

2006-2009 **Officer,** IAF, IDF
Served as a commander in several positions, including intelligence officer course.

2005 **Certified Tae-Kwon-Do Instructor,** "Ahi Yehuda" Association, Jerusalem

Publications

Refereed Conference Papers:

(1) R. Ben-Hur and S. Kvatinsky, "Memristive Memory Processing Unit (MPU) Controller for In-Memory Processing," IEEE International Conference on the Science of Electrical Engineering (ICSEE), November 2016 (in press).

(2) R. Ben-Hur, N. Talati, and S. Kvatinsky, "Algorithmic Considerations in Memristive Memory Processing Units (MPU)," Proceedings of the International Cellular Nanoscale Networks and their Applications (CNNA), August 2016 (in press).

(3) R. Ben-Hur and S. Kvatinsky, "Memory Processing Unit for In-Memory Processing," Proceedings of the IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), pp. 171-172, July 2016.

Selected Talks:

(4) R. Ben-Hur and S. Kvatinsky, “Memory Processing Unit (MPU) for In-Memory Processing,” The 25th International Conference on Parallel Architectures and Compilation Techniques (PACT), September 2016.

(5) R. Ben-Hur and S. Kvatinsky, “Processing within a Memristive Memory Using Memory Processing Unit,” ChipEx, The major annual event of the Israeli microelectronics industry, May 2016.

(6) R. Ben-Hur and S. Kvatinsky, "Processing within a Memristive Memory," workshop on Memristor Technology, Design, Automation and Computing (memTDAC), HiPEAC conference, January 2016.

Posters:

(7) R. Ben-Hur and S. Kvatinsky, "Processing within a Memristive Memory," Proceedings of the International Workshop on Emerging Memory Solutions, DATE Conference, March 2016.

(8) N. Talati, R. Ben-Hur, N. Wald, and S. Kvatinsky, “Data Storage and Processing within Memristive Memory Processing Units (MPUs),” Intel Collaborative Research Institute - Computational Intelligence (ICRI-CI), May 2016.

Technical Reports:

(9) R. Ben Hur, N. Wald, N. Talati, and S. Kvatinsky, “Latency Optimized Mapping of Logic Functions for Memristor Aided Logic (MAGIC),” CCIT Technical Report #908, Dec. 2016.