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SPECIAL ISSUE PAPER

Analysis of the row grounding technique in a memristor-based crossbar array

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SUMMARY

Using memristive devices within a crossbar array could pave the way for memories with higher density and speed than state-of-the-art Flash memory, while maintaining relatively low energy. However, memristive crossbar arrays have great difficulty distinguishing logical states because of sneak path currents. The row grounding technique eliminates the sneak path effect, allowing reliable sampling of the memristor state. In this paper, we analyze the row grounding technique and propose several methods and constraints for the design of memristive crossbar arrays. When the row grounding technique is used for these arrays, our analysis shows that increasing the number of rows can help reduce read latency and energy, in contrast to the case of capacitive memory arrays. Simulation results confirm the theoretical analysis proposed in this paper.

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KEY WORDS: resistive RAM; memristor; crossbar; sneak path; row grounding

1. INTRODUCTION

The memristor [1, 2] (memory resistor) is a passive, two-terminal, nonvolatile electrical device with varying resistance that changes as a function of its voltage. The unique properties of the memristor can be beneficial for many applications, such as threshold switch [3], dynamic load [4] and memory, which is considered the primary application for these devices. Resistive random-access memory [5–11] is one interesting type of memristive device [12]. Unlike standard nonvolatile memory cells such as Flash, resistive random-access memory can be smaller, vertically stacked (three-dimensional crossbar array structures [13, 14]), with lower energy and lower read/write latency [15–17]. The crossbar configuration has many benefits: Its structure has the highest memory density in comparison with other structures [18–21], and it can be fabricated above the Complementary metal-oxide-semiconductor (CMOS) logic circuitry, which allows superior memory capacity and reduced read latency. One drawback of the memristor crossbar is the existence of sneak path currents, which inhibit accurate sensing of the memory cell resistance. Although the sneak path problem is well established [22–26], no satisfactory solution has been found. One possible solution is row grounding [22], where unselected rows are grounded to reduce sneak paths and increase sensing accuracy.

Previous works show different approaches to overcoming the sneak path problem, for example, by adding additional cell elements such as 1D1R [27], 1T1M [28], and antiserial memristive elements [29]. While handling sneak paths in a passive crossbar using row or column grounding techniques has been shown to yield poor noise margins [26], another analysis has shown that adjusting the sense circuit load can improve these margins [30]. In this paper, we propose an analytical model for a read operation row

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grounding method to evaluate different trade-offs between array size, read latency, energy, and operating voltage levels. We also offer further optimization of the sense circuit's load resistance to improve the noise margins. Our analysis shows that adding rows to a row-grounded memristive memory crossbar can reduce both read latency and energy. This is in contrast to charge-based memory technologies (e.g., static random-access memory or dynamic random-access memory), where adding rows does not have this effect. The proposed analysis is evaluated using a practical memristor model based on the ferroelectric memristor [31].

We also present the Crossbar Designer Tool, which provides crossbar size constraints, optimal read voltage, read latency, and energy to assist in designing the appropriate sensing circuitry. This tool, available at [32], simplifies the design of a generic memristive crossbar network.

The remainder of this paper is organized as follows. In Section 2, the crossbar array structure and the sneak path phenomenon are described. Section 3 presents an analysis of a 1-by-1 (single cell) memory array. Section 4 shows a circuit analysis of an M-by-N memory array. Section 5 presents a read latency analysis of an M-by-N memory array, and Section 6 discusses the constraints on such an array. In Section 7, we show the excellent match between simulation results and the analysis. The paper is summarized in Section 8.

2. SNEAK PATH IN A MEMRISTIVE CROSSBAR ARRAY

A crossbar consists of two perpendicular metal wire layers, where every crosspoint forms a single memristive device. This crossbar stores data within the memristors in the form of resistance [33]. The rows of the crossbar are word lines, and the columns are bit lines. A popular scheme for write operations is the half-select method: A voltage V_{write} is applied to the word line of the selected memristor, and the ground is connected to its bit line. A voltage $V_{write}/2$ is applied to all other rows and columns to prevent writing unselected cells [34]. Typically, the voltage required to perform a write operation is much higher than that required for a read operation.

The stored data are read by measuring the resistance of the selected memristor. A sense amplifier and a reference resistor R_{ref} are connected to each column to sample the output voltage and determine the stored value. The sense amplifier adds load capacitance for each bit line (C_{SA}), as illustrated in Figure 1. A voltage V_{read} is applied to a selected row, and the voltage across an external reference

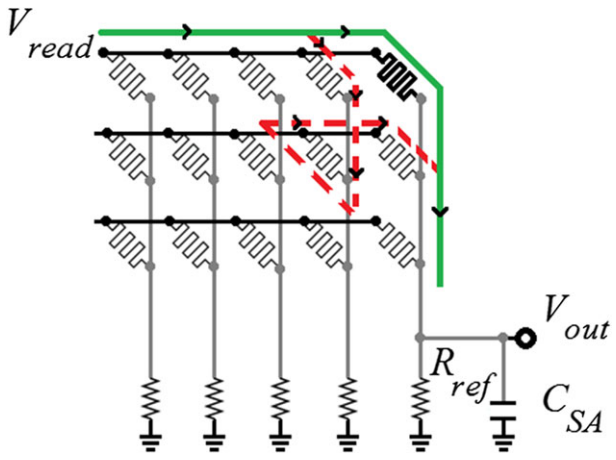

Figure 1. Sneak path demonstrated in a 3-by-5 memristive crossbar array performing a read operation. The cell marked bold is selected, its row is connected to a voltage, V_{read}, and its column is connected to a reference resistor, R_{ref}, and a sense amplifier with capacitance C_{SA}. To avoid clutter, only the capacitance at the input of the sense amplifier on the last column of the crossbar is shown. The voltage measured by the sense amplifier determines the state of the selected memristor. The green (solid) current path is the desired one for a correct measurement of the selected memristor's resistance. The red (dashed) current path is one example of an undesired parallel current path (sneak path), reducing the effective resistance of the selected cell and increasing current through R_{ref}, which leads to a possible faulty measurement of the selected memristor's state by the sense amplifier. [Colour figure can be viewed at wileyonlinelibrary.com]

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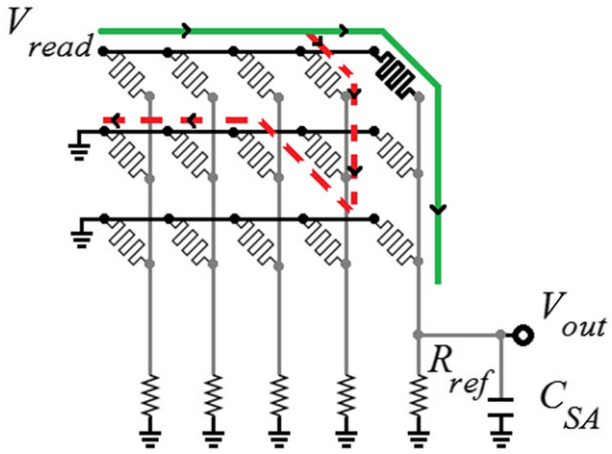

Figure 2. A 3-by-5 row-grounded memristive crossbar array performing a read operation: The cell marked bold is selected, its row is connected to a voltage V_{read}, while all other rows are grounded. This way, sneak path currents are completely eliminated. Each column is connected to a reference resistor R_{ref} and a sense amplifier with capacitance C_{SA}. This configuration allows sampling the resistance of the selected memristor by the sense amplifier measured voltage. To avoid clutter, only the capacitance at the input of the sense amplifier on the last column of the crossbar is shown. [Colour figure can be viewed at wileyonlinelibrary.com]

resistor connected to the column in series is measured by the sense amplifier. The resistive nature of a memristor-based crossbar array leads to difficulties in accurately sensing the stored value in large arrays, because of sneak path currents. As illustrated in Figure 1, a sneak path current (marked in dashed red) lowers the effective resistance of the measured upper right memristor. This crossbar configuration can be modeled as many resistors that are connected in parallel to the memristor [22]. In larger crossbars, the greater number of sneak paths makes it even more difficult to distinguish between the stored values.

Various techniques have been proposed to reduce the sneak path effect, including multistage reading, diode gating, and transistor gating [22, 27–29]. In this paper, we focus on the row grounding technique, where unselected rows are grounded, as shown in Figure 2. The sneak path is eliminated because, unlike in a regular crossbar, the sneak path currents are directed to the ground and do not affect the sense amplifier. The row grounding solution is easy to implement and does not require additional circuit elements. This technique also allows the reading of multiple bits from the same row simultaneously, as the memristors are isolated by the grounding. The downside of the row grounding technique is a decrease in the output voltage, because of parallel connected memristors in each column, as further explained in Section 4.

3. CIRCUIT ANALYSIS OF A 1-BY-1 MEMORY CELL

In this section, an analysis of the read operation of a simple memory array consisting of a single cell is presented. Understanding the 1-by-1 memory cell provides a solid base for the analysis of the general M-by-N array. During the read operation of a single memristor memory cell, the cell consists of a voltage source, V_{read}, a memristor device with varying resistance, $R_{memristor}$, a reference resistor with a fixed resistance R_{ref}, and a sense amplifier with an input capacitance C_{SA}. The sensed voltage is the voltage across the reference resistor, V_{out}, as shown in Figure 3. Because the read voltage is lower than the write threshold, the resistance of the selected memristor remains unchanged during the read operation and can be equivalently modeled by a constant valued resistor. The R_{off} parameter is the maximal resistance of the device, while the R_{on} parameter is its minimal resistance, as measured and illustrated in [31] (figure 1a). To optimize the distinction between the different states of stored data (in multilevel cells), the resistance of the reference resistor is chosen to be

$$R_{ref} = \sqrt{R_{off} \cdot R_{on}}, \tag{1}$$

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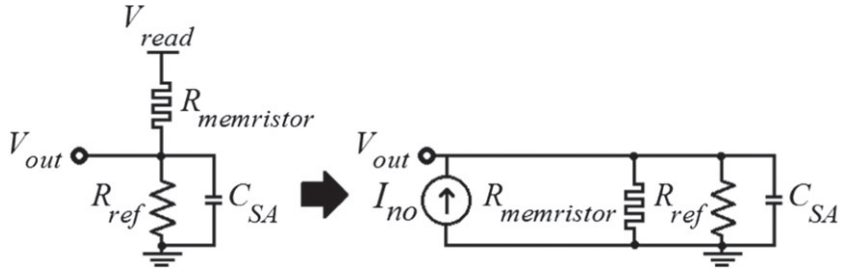

Figure 3. Equivalent circuit for a 1-by-1 memristor memory cell, connected to a reference resistor R_{ref} and a sense amplifier with input capacitance C_{SA}. This configuration is a voltage divider between $R_{memristor}$ and R_{ref}. Using Norton's theorem, we can convert the 1-by-1 memristor memory cell's equivalent circuit to a more convenient form for timing calculations, where $I_{no} = V_{read}/R_{memristor}$.

as in [24]. Under these assumptions, a 1-by-1 memristor cell has two possible and easily distinguishable memristor states:

$$V_{out} = \frac{R_{ref}}{R_{memristor} + R_{ref}} \cdot V_{read} \underset{Vread=1V}{=} \begin{cases} 0.054V, \ R_{memristor} = R_{off} \\ 0.945V, \ R_{memristor} = R_{on} \end{cases}. \tag{2}$$

For a ferroelectric memristor [31], the following values are used: $V_{read} = 1V$, $R_{on} = 150k\Omega$, $R_{off} = 45M\Omega$, $R_{ref} = 2.6M\Omega$. As this work mostly discusses the read operation without considering the dynamic behavior of the memristor while switching, the ferroelectric memristor is utilized as a varying resistor with two resistance states. Additionally, a sense amplifier with settling time of $T_{settling} = 150ps$ and $C_{SA} = 5fF$ is used. The sense amplifier parameters have been selected to fit the Analog Devices Single-Supply SiGe Comparator ADCMP572 [35].

It is crucial that V_{read} is low enough so as not to disturb the memristor's state upon reading or harm the memristors' durability. In this paper, it is assumed that $V_{read} = 1V$ is sufficient for this purpose and to ensure that the lifetime of the memory is limited by write operations.

The 1-by-1 memristor cell has a read operation latency of 1.71 ns, and the sense amplifier sample settling time is determined by $2.2 \cdot \tau = 2.2 \cdot R_{eq1\times1} \cdot C_{SA}$ (the voltage rise time from 10% to 90% of the steady-state value in an resistor–capacitor [RC] circuit). Only the R_{on} state is considered for τ, where C_{SA} needs to be charged to a higher voltage, while if the memristor resistance is R_{off}, the output voltage stays low. The equivalent resistance, $R_{eq1\times1}$, is

$$R_{eq1\times1} = R_{on} \parallel R_{ref}. \tag{3}$$

Furthermore, a settling time of $T_{settling}$ is required for a proper operation of the sense circuit (settling time of the sense amplifier). The time for a read operation is therefore

$$T_{read} = T_{settling} + 2.2 \cdot \tau = 1.71ns. \tag{4}$$

4. CIRCUIT ANALYSIS OF AN *M*-BY-*N* ARRAY

Following the single memristor array analysis, a method for analyzing an M-by-N memristor crossbar array is presented. Assuming only two logical states for memristors, 'off' and 'on' states, an M-by-N memristor crossbar has $2^{M \cdot N}$ possible states, where each state produces different sneak path currents. Using the row grounding technique allows us to completely eliminate sneak path currents with the inconvenience of lowering the output voltage, thus making it difficult to distinguish between the states of the selected memristor. However, because the read voltage is sufficiently low, the memristors in the grounded rows are not stressed, and the durability of the cells is not significantly affected. The model, which is presented in the following paragraphs, enables the formulation of a clear constraint on the crossbar size and accurate calculations of the crossbar's parameters.

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Table I. Memristor state scenarios.

Scenario	Set X	Desired output voltage	Set Y	Output voltage	Notes
Scenario A	'on'	High	'on'	Lower (135mV*)	Worst case
Scenario B	'on'	High	'off'	High (702mV*)	Best case
Scenario C	'off'	Low	'on'	Low (0.54mV*)	Best case
Scenario D	'off'	Low	'off'	Higher (6.95mV*)	Worst case

* These values refer to the simulation results shown in Figure 5. Note that the 'Higher' notation in the output voltage of scenario D relates to the output voltage of scenario C and the 'Lower' notation in the output voltage of scenario A relates to the output voltage of scenario B.

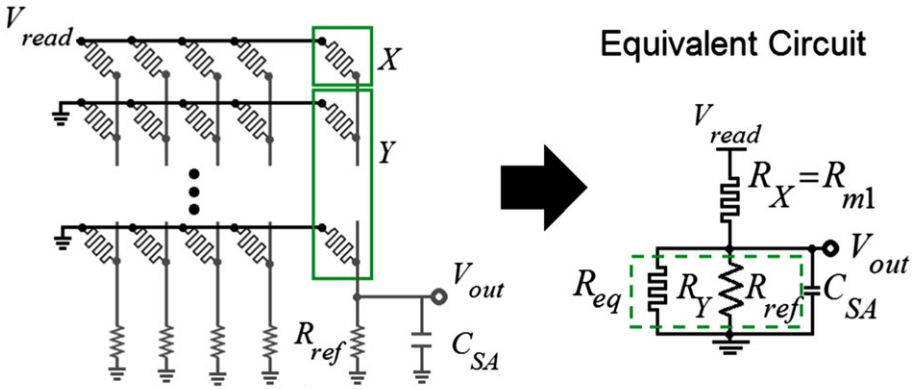

Figure 4. An M-by-5 memristor crossbar array and its equivalent circuit. The upper right memristor is marked by X, and all other memristors in its column are marked by set Y. There are four possible edge case scenarios for the output voltage value V_{out}, depending on the resistance values of X and Y. These scenarios are shown in Table I, and the simulation results for them are shown in Figure 5, where, however, $N = 7$. [Colour figure can be viewed at wileyonlinelibrary.com]

Our method considers all edge cases, constituting best and worst case scenarios. We define X as the selected memristor and set Y as all other memristors in the same column and having the same logical values, as illustrated in Table I and Figure 4. The reference resistor R_{ref} is connected in parallel to all of the memristors in set Y. When all memristors in set Y are in the 'on' state, the output voltage is significantly lowered. When all set Y memristors are in the 'off' state, the output voltage is only slightly lowered, as can be seen in Figure 5 and Table I. Therefore, scenarios B and C are the best case scenarios while scenarios A and D are the worst case scenarios in terms of output voltage distinction. Figure 5 shows these scenarios as simulated on a 7-by-7 memristor crossbar array. The read voltage is $V_{read} = 1V$, and the capacitance of the sense amplifier is $C_{SA} = 5fF$, similar to the single cell configuration. This crossbar was designed and simulated using Cadence Virtuoso.

To distinguish between the 'on' and 'off' states of the selected memristor, the sense circuit that measures the voltage drop on R_{ref} must have a minimal voltage offset, given by

$$V_{offset} < \frac{V_{Out,scenario\,A} - V_{Out,scenario\,D}}{2} = \frac{\Delta V_{out}}{2}. \tag{5}$$

For large crossbar arrays, the resistance of the crossbar wires cannot be ignored. In our evaluation, we assume that the interconnect resistance, R_{wire}, between each pair of adjacent junctions is 1.25Ω [36]. To achieve a simpler modeling of the sneak path effect, it is possible to ignore R_{wire} as long as the following condition is satisfied:

$$R_{on} \gg R_{wire} \cdot (N + M - 1) \cong R_{wire} \cdot (N + M), \tag{6}$$

where $R_{wire} \cdot (N + M - 1)$ is the wire resistance of the entire path when performing a read operation on memristor R_X.

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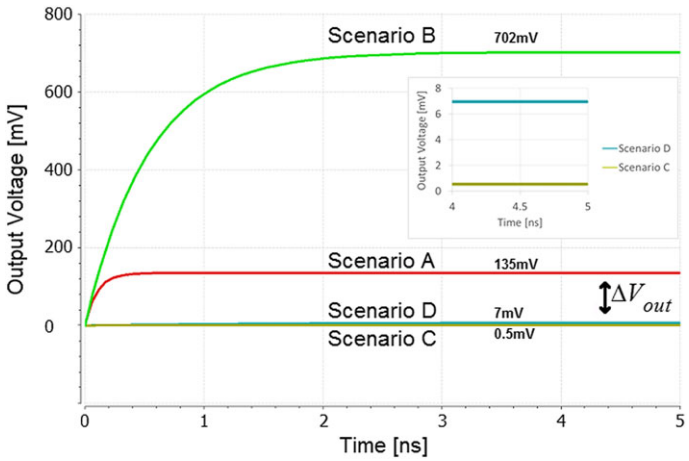

Figure 5. Spice simulation results of output voltages of a 7-by-7 crossbar with ferroelectric memristors. Scenarios A and D are the worst case scenarios in terms of output voltage distinction. Therefore, the sense amplifier's minimal voltage offset, V_{offset}, must be lower than $\Delta V_{out}/2$ as determined in (5). The read voltage is $V_{read} = 1V$, and the sense amplifier's capacitance is $C_{SA} = 5fF$. Inset shows a zoom on scenarios C and D. [Colour figure can be viewed at wileyonlinelibrary.com]

This condition is based on the fact that if the crossbar wire resistance is significantly lower than R_{on}, the voltage drop across the wires is substantially lower than the voltage drop on the memristor. This condition does not apply on large crossbar arrays or low R_{on} devices. For the ferroelectric memristor, the upper limit for $N + M$ is approximately 12,000. When the condition in (6) is satisfied, an accurate modeling of the crossbar can be achieved in a few steps. The voltage divider shown in Figure 4 is between R_{m1} (marked as X) and R_{ref}, parallel to all other memristors in that column (marked as Y). To analyze the worst and best case scenarios under $R_{m1} = R_{on}$, as seen in the first two rows in Table I, we define the equivalent resistance of the Y set memristors as

$$R_Y = R_{m2} \parallel R_{m3} \parallel ... \parallel R_{mM} = \begin{cases} \dfrac{R_{on}}{M-1} & \text{worst case} \\ \dfrac{R_{off}}{M-1} & \text{best case} \end{cases}. \tag{7}$$

The equivalent resistance, R_{eq}, is composed of parallel resistances: the reference resistance R_{ref} and the resistance R_Y of the $M - 1$ resistors on the same column of the selected memristor. The output voltage is therefore

$$V_{out} = V_{read} \cdot \frac{R_{eq}}{R_X + R_{eq}}, \quad R_{eq} = R_{ref} \parallel R_Y. \tag{8}$$

When the condition in (6) is fulfilled, we can regard the whole crossbar as a symmetric grid. Hence, this analysis applies to any memristor in the crossbar, regardless of its row/column position. To maximize ΔV_{out}, it is necessary to choose a corresponding R_{ref}. The optimal R_{ref} is obtained by extracting the maximum from ΔV_{out} by solving

$$\frac{\partial(\Delta Vout)}{\partial R_{ref}} = 0, \tag{9}$$

which gives

$$R_{ref} = \frac{\sqrt{R_{on} \cdot R_{off}}}{M}, \tag{10}$$

confirming that the number of columns does not affect V_{out}. As more rows M are added to the crossbar, the output voltage V_{out} decreases as a result of the decrease in R_{ref}, R_Y, and thus R_{eq}, as determined in

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(7), (8), and (10). While the output voltages of scenarios C and D in Table I are close to 0 even with a small number of rows, the output voltages of scenarios A and B go down quickly, lowering ΔV_{out} and constraining V_{offset}, as determined in (5).

For crossbars with longer wires, the wire inductance must be taken into account. The wire inductance turns the circuit from an RC tree to an RLC tree. However, the inductance does not necessarily affect the read latency. Assuming a relatively low inductance, the signal will rise a bit more slowly at first but will reach the required voltage before the read time of $2.2 \cdot R \cdot C$ (the voltage rise time from 10% to 90% of the steady-state value in an equivalent RC circuit). As determined in [37], the equivalent Elmore delay for RLC circuits is relatively similar to the RC delay. The primary downside of the inductance is that the signal will have an overshoot and ripple, and their magnitude depends on the exact values of the wire inductance. To summarize, RLC modeling of the crossbar array will not contribute to the read latency as compared with the proposed RC model.

In this section, we analyzed a single memristor in an M-by-N crossbar, but the analysis applies to all memristors in the selected row, meaning that the entire row can be read simultaneously, hence reducing the amount of energy per bit while maintaining all other parameters unchanged (the energy per bit is the read operation energy, divided by the number of the bits in the selected row).

5. READ LATENCY OF AN M-BY-N CROSSBAR ARRAY

In an M-by-N crossbar, the read latency expression in (4) cannot be used because of the intrinsic wire resistances and capacitances that have to be considered, as shown in Figure 6. To provide a sufficient approximation for the crossbar latency, the RC tree Elmore delay formula [37–40] is used, where i is an index that covers each capacitor in the circuit and R_k represents the cumulative resistance from the

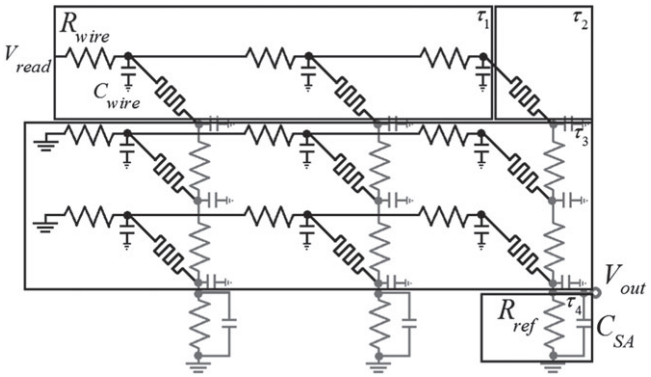

Figure 6. 3-by-3 memristive crossbar with wire resistance and capacitance modeling. Each column is connected to a reference resistor R_{ref} and a sense amplifier with capacitance C_{SA}. In order to simplify the crossbar delay calculation, the crossbar has been marked with four rectangles $\tau_1 - \tau_4$, which are calculated separately using the Elmore delay formula (12).

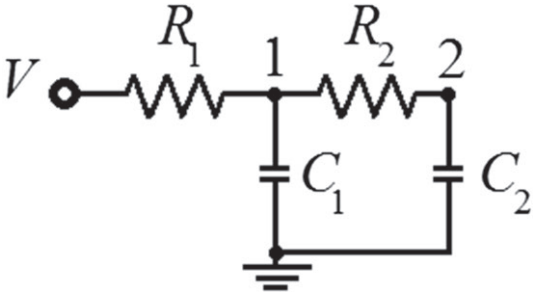

Figure 7. Example circuit for a simple resistor–capacitor circuit, $\tau_1 = T_{D1} = R_1 \cdot C_1$, $T_{D2} = (R_1 + R_2) \cdot C_2$ and the total Elmore delay to node 2 is $\tau_2 = T_{D1} + T_{D2}$.

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input to node i passing through all nodes k with k from 1 to i. Simply put, when calculating the total delay from an input to node i, we must consider all previous nodes in the path from the input to node i, and for every previous node, we must consider all resistances R_k in the path from the input to that node. T_{Di} is the delay contributed by node i as illustrated in Figure 7.

$$T_{Di} = C_i \cdot \sum_{k=1}^{i} R_k. \tag{11}$$

R_X is chosen as R_{on} because the bottleneck of the read operation in terms of read latency is charging C_{SA}. When sampling a memristor that is set to R_{off}, the sense amplifier is charged to low voltage. The charging time is substantially higher when the resistance of the memristor is R_{off} ($R_{off} \gg R_{on}$), but the steady-state value of the output voltage is very close to the initial condition. Therefore, as can be seen in Figure 5, it is sufficient to sample the voltage correctly after scenarios A and B settle. In these scenarios R_x is equal to R_{on}. If within the read operation interval C_{SA} remains discharged, then R_X is in the 'off' state. τ_i represents the total Elmore delay ΣT_{Di} as illustrated in Figure 6. The corresponding expressions for the read latency are

$$\begin{aligned}
\tau_1 &= C_{wire} \cdot R_{wire} \cdot \frac{(N+1) \cdot N}{2}, \\
\tau_2 &= C_{wire} \cdot (R_{on} + N \cdot R_{wire}), \\
\tau_3 &= C_{wire} \cdot (R_{on} + N \cdot R_{wire}) \cdot \left(ln(M) + 0.577 + \frac{1}{2 \cdot M} - \frac{1}{12 \cdot M^2} - 1 \right), \\
\tau_4 &= C_{SA} \cdot (R_{eq} \parallel ((M + N - 1) \cdot R_{wire} + R_{on})),
\end{aligned} \tag{12}$$

where τ_1 is the row delay, τ_2 is the delay of the selected memristor, τ_3 is the approximation of the column delay using the partial sum of harmonic series (0.577 is the Euler–Mascheroni constant) [41], and τ_4 is the sense circuit delay, as illustrated in Figure 6. The calculation method is detailed in Appendix A. Finally, the total read latency for an M-by-N crossbar is

$$T_{read} = T_{settling} + 2.2 \cdot \sum_{i=1}^{4} \tau_i. \tag{13}$$

When the rule in (6) is kept, τ_3 and τ_4 are the dominant factors in the set $\{\tau_i\}, i = \{1, 2, 3, 4\}$. With the increase in the number of rows, the read latency shortens because of the decrease of R_{eq}, which is dominant in τ_4. By adding more rows, τ_3 becomes dominant, and the read latency increases, but not as

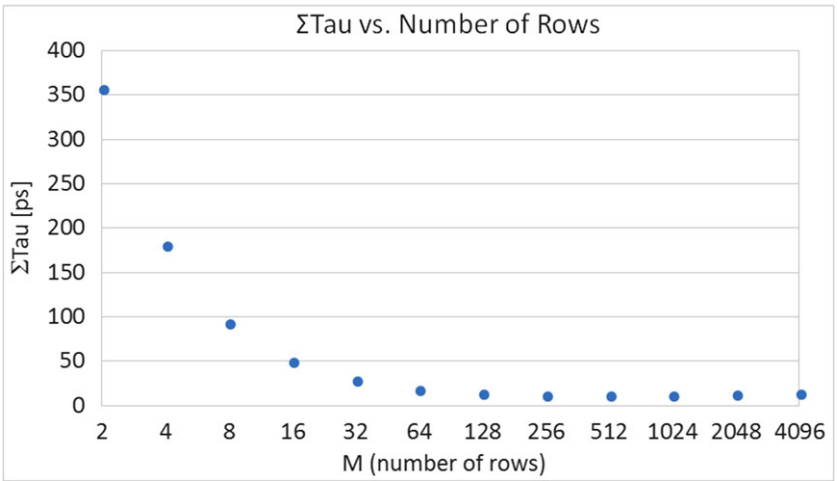

Figure 8. The memristive crossbar latency $\sum_{i=1}^{4} \tau_i$ for different numbers of rows, for $N = 128$ columns. The read latency decreases as the number of rows increases because of the decrease in τ_4. In this example, when the number of rows reaches 1024, τ_3 becomes dominant, and the read latency slowly increases with the number of rows. R_{ref} is selected according to (10), $R_{wire} = 1.25\Omega$ and $C_{wire} = 0.01fF$. [Colour figure can be viewed at wileyonlinelibrary.com]

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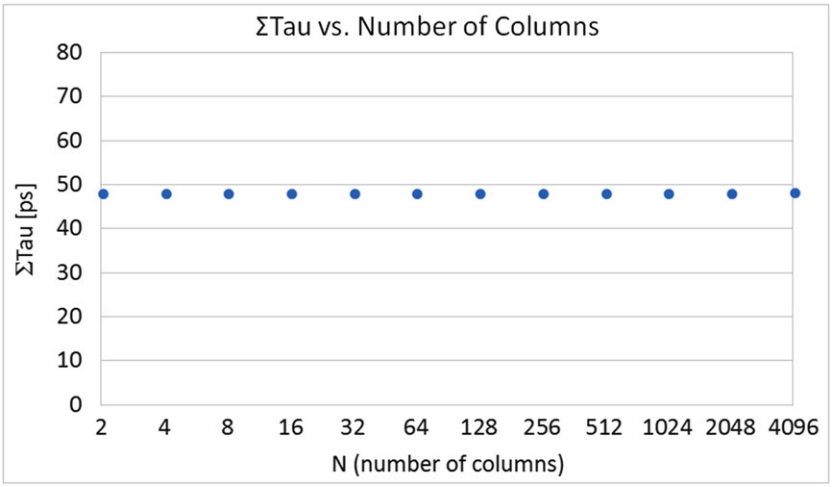

Figure 9. The memristive crossbar latency $\sum_{i=1}^{4} \tau_i$ for different numbers of columns, for $M = 16$ rows. The read latency is negligibly affected by the number of columns. R_{ref} is selected according to (10), $R_{wire} = 1.25\Omega$ and $C_{wire} = 0.01fF$. [Colour figure can be viewed at wileyonlinelibrary.com]

much, as shown in Figure 8. R_{on} and R_{eq} are never multiplied by N; therefore, increasing the number of columns has a negligible effect on the total read latency, as shown in Figure 9. Additionally, for a larger crossbar, the sense circuit capacitance becomes negligible, while the wire capacitance becomes significant; therefore, the wire capacitance must be considered for larger crossbars. The energy of the circuit read operation of N memristors can be evaluated as the energy of each column E_{column} times N, where each column consists of M memristors, R_X is chosen to be R_{on} to address the worst case scenario in terms of energy, and a sense amplifier with energy of E_{SA} is taken into account. We have

$$E_{total} = N \cdot (E_{column} + E_{SA}) = N \cdot \frac{{V_{\mathrm{Read}}}^2}{R_{on} + R_{eq}} \cdot T_{read} + N \cdot \frac{1}{2} \cdot C_{SA} \cdot {V_{out}}^2. \tag{14}$$

While both R_{eq} and V_{out} inversely depend on the number of rows M as determined in (7), (8), and (10), the effect on the energy is stronger through V_{out} because of the power of 2, meaning that the overall energy decreases with the increase in M. Note that, in this configuration, R_{ref} is optimized to maximize the readout margin ΔV_{out} (as determined in (9) and (10)) and is a function of the number of rows. This approach allows us to fairly compare different optimized designs, as can be seen in Section 7.

6. MEMRISTOR-BASED CROSSBAR ARRAY CONSTRAINTS

The number of rows and columns of the memristor-based crossbar array is constrained also by choices of V_{read}, V_{write} and the current driver of the crossbar. In this section, we also discuss the influence of wire resistance R_{wire} on crossbar size.

6.1. The current driving constraint

The crossbar dimensions are limited by the amount of current it consumes during the write cycle. This current is provided by an external driving circuit, which must comply with the maximum current draw of the crossbar.

In the case of the ferroelectric memristor, the current consumption during the write cycle is composed of two elements: the current that goes through the memristor we intend to write , $I = \frac{Vwrite}{R_{on}}$, and the current that flows through unselected memristors, $I = \frac{(M+N-2)\cdot Vwrite/2}{R_{on}}$. In case of current consumption, the memristors resistance in the worst case scenario is set to be R_{on}, and the voltage drop on the unse-

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lected memristors is $Vwrite/2$, because the half select method is used [34]. Note that current flows from both the selected row to the unselected columns and from the unselected rows to the selected column, resulting in $M+N-2$ current paths. The maximum cumulative current is therefore $I_{max} = (\frac{M+N-2}{2}+1)\cdot \frac{Vwrite}{R_{on}}$, resulting in a constraint for the number of rows and columns, given by $N+M < 2\cdot I_{max}\cdot \frac{Ron}{Vwrite}$.

A typical power supply for L1 cache using 65 nm CMOS process [42] can provide up to $68\frac{mW}{V}$. Assuming that the ferroelectric memristor crossbar has the same driver as the mentioned L1 cache, for V_{write} of $2.25V$, the crossbar dimensions are limited by $M+N < 4000$. With the current driver capabilities, the dominant parameter for determining the crossbar size limitations is determined by R_{on}. Higher R_{on} devices allow larger crossbars for the same current driving capabilities.

6.2. The write voltage constraint

In large crossbars, the wire resistance cannot be ignored because the write voltage used for writing a cell is divided between the selected memristor and the wires. If the writing voltage is too high, other memristors might also be written. If the writing voltage is too low, the selected memristor will not be written. The writing voltage should be set so that the voltage drop on the selected memristor is higher than the voltage threshold V_T of the selected memristor. The worst case scenario is when $R_X = R_{on}$ and the total wire resistance in the read path is $(N+M-1)\cdot R_{wire}$. In this case, the voltage drop on the wires is maximal, as the top right memristor has N nodes to its left and $M-1$ on the path to ground and, therefore,

$$V_{write} > V_T \cdot \frac{R_{on} + R_{wire}\cdot(N+M-1)}{R_{on}}. \tag{15}$$

As a write technique, we adopt the half-select method [34]. In this method, we assign $V_{write}/2$ to all rows and columns in the crossbar except for the selected memristor's row and column to prevent unwanted writing to other memristors. The applied voltage $V_{write}/2$ must be lower than the minimum V_T. The memristor most susceptible to this effect is the one at the lower left of the crossbar. The path to this memristor has the lowest wire resistance because the voltage source and the sense circuit are in physical proximity. Therefore, the constraint on the writing voltage is

$$V_{write} < 2\cdot V_T. \tag{16}$$

From (15) and (16), we get that the constraint on the array size is

$$\frac{R_{on}}{R_{wire}}\left(\frac{1-A}{A}\right)+1 > N+M, \tag{17}$$

where $A \triangleq V_T/V_{write}$ and its values range between 0.5 and 1.

The exact value of A is determined by the circuit designer; increasing the size properties of the array $(M+N)$ requires lower A and trades off with the noise robustness of the memory, as having more rows M leads to a lower output voltage V_{out} as determined in (8). For example, when using the ferroelectric memristor with $A = 0.6$, the $N+M$ constraint is approximately $N+M < 80,000$. Note that the constraint in (17) is well above the limits of the model presented in this paper, because it is assumed that $R_{on} \gg (N+M)\cdot R_{wire}$, as determined in (6). For example, when using the rule in (6) for the ferroelectric memristor, the constraint is approximately $N+M < 12,000$.

It is possible to expand all the constraints shown in this section with a standard resource sharing technique (similar to the method shown in [43, 44]), doubling the number of rows while still staying within the constraints mentioned previously. This technique does not affect output voltages, read latencies, or the energy of the network, and it does not cost additional sense amplifiers.

6.3. The read voltage constraint

The read voltage in the crossbar has two effects on the system: Lower read voltage leads to lower energy as determined in (14), and higher read voltage results in larger ΔV_{out} and allows the use of

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sense circuits with higher V_{offset} as determined in (5). To prevent resistance drift of a memristor while reading, the designer must confirm that the read voltage does not surpass the voltage threshold V_T. The read voltage is constrained by the write current of the memristor multiplied by the resistance of the memristor, the wire resistance, and R_{eq}, where the worst case scenario is when $R_{memristor} = R_{on}$ and $R_{wireTotal} = (N + M - 1) \cdot R_{wire}$. When the read voltage is higher than this constraint, the memristor will be written, and therefore,

$$V_{read} < (R_{on} + R_{wire} \cdot (N + M - 1) + R_{eq}) \cdot \frac{V_T}{R_{on}}. \tag{18}$$

Note that the only physical constraint on the minimal read voltage is the sensitivity of the sense circuit V_{offset}.

In order to design an optimal crossbar in terms of energy, latency, and readout margin, the designer is advised to select circuit parameters appropriately. First, the maximal number of rows M is deduced from the following parameters: the offset voltage of the sense amplifier as determined in (5), the memristor resistances and the input voltage of the crossbar for the read operation as determined in (7) and (8).

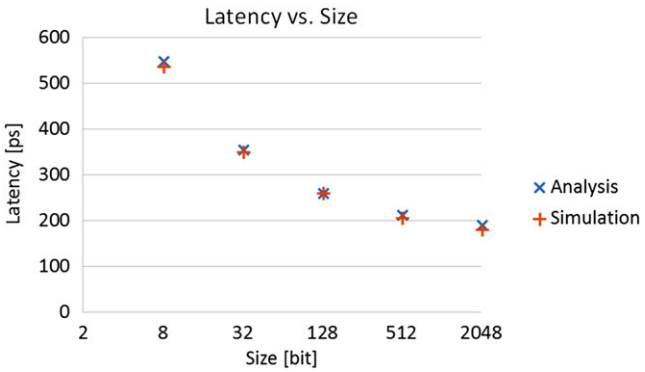

Figure 10. Read latency of an $\frac{N}{2} \times N$ memristive crossbar for different array sizes as determined in (13). Unlike capacitive memories, increasing the size of the crossbar can decrease the read operation latency until a certain point after which it increases again (Figure 8). V_{read} is chosen to be minimal using (5) and (8), R_{ref} is selected according to (10), $R_{wire} = 1.25\Omega$, and $C_{wire} = 0.01fF$. [Colour figure can be viewed at wileyonlinelibrary.com]

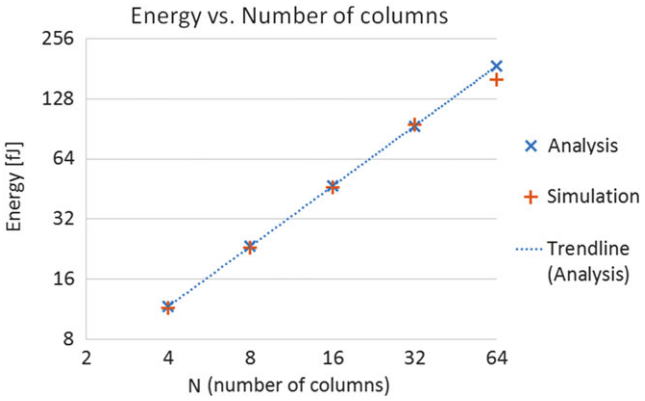

Figure 11. Energy of memristive crossbar for different numbers of columns. The read operation energy is linear with the number of columns as determined in (14). The number of rows is $M = 4$, $V_{read} = 1V$, R_{ref} is selected according to (10), $R_{wire} = 1.25\Omega$ and $C_{wire} = 0.01fF$. [Colour figure can be viewed at wileyonlinelibrary.com]

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Once the choices for M and V_{read} have been made, the number of crossbar columns N is next. The choice of N trades off energy and crossbar size as determined in (14). A tool [32] was created to assist in designing the appropriate crossbar parameters, based on this methodology.

7. COMPARISON WITH SIMULATION

To verify the proposed analysis, memristor crossbar simulations, including wire resistances and capacitances, were performed using Cadence Virtuoso. The simulations demonstrate different trade-offs between the crossbar size and other parameters such as latency, energy, and noise margins. Figure 10 shows how the read latency decreases as the crossbar grows larger (for an $\frac{N}{2}\times N$ crossbar). This decrease comes from the increase in the number of rows, while increasing the number of columns has no effect on the read latency, as determined in (12). Figure 11 shows that the energy increases linearly with the number of columns, as determined in (14). Note that the energy per bit remains constant. Figure 12 shows a slight decrease of energy when increasing the number of rows, although, as shown in Figure 13,

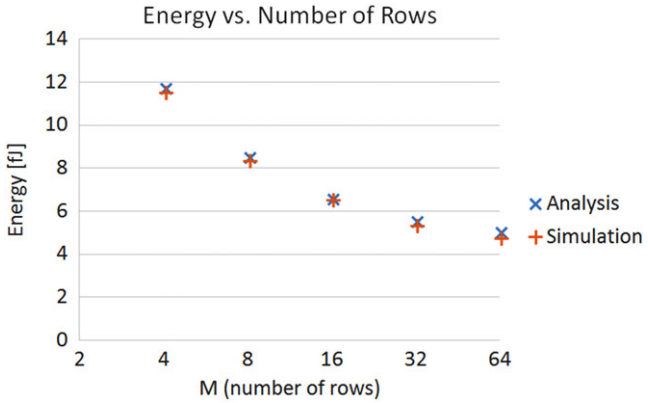

Figure 12. Energy of memristive crossbar for different numbers of rows. As an increase in the number of crossbar rows reduces the output voltage, as determined in (8), and the read operation latency, as shown in Figure 8, the energy of the read operation is also reduced, according to (14). The number of columns is $N = 4$, $V_{read} = 1V$, R_{ref} is selected according to (10), $R_{wire} = 1.25\Omega$ and $C_{wire} = 0.01fF$. Note that modifying the number of rows affects the energy due to the changes in the output voltage V_{out} and in the equivalent resistance R_{eq}, both appearing in (14). The decrease in V_{out} dominates the reduction in energy through the power of 2 in the second term of the right-hand side of (14). [Colour figure can be viewed at wileyonlinelibrary.com]

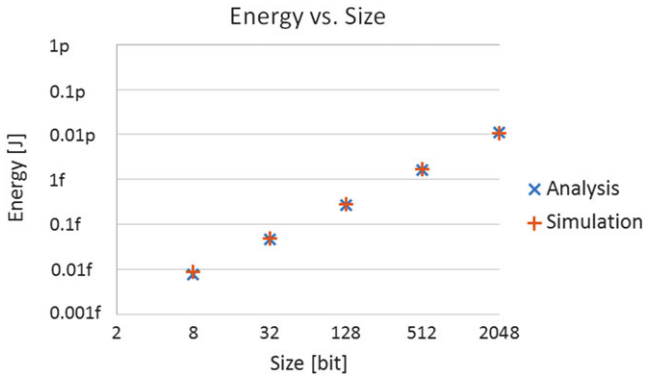

Figure 13. Energy of an $\frac{N}{2}\times N$ memristive crossbar for different array sizes as determined in (14). V_{read} is chosen to be minimal using (5) and (8), R_{ref} is selected according to (10), $R_{wire} = 1.25\Omega$ and $C_{wire} = 0.01fF$. Note that modifying the number of rows affects the energy due to the changes in the output voltage V_{out} and in the equivalent resistance R_{eq}, both appearing in (14). The increase in the number of columns dominates the increase in energy through the linear dependence on N in the first term of the right-hand side of (14). [Colour figure can be viewed at wileyonlinelibrary.com]

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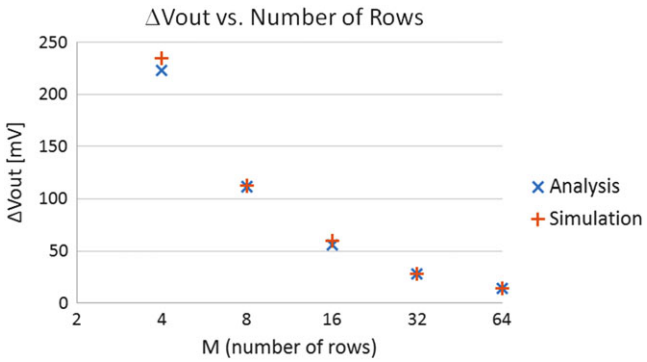

Figure 14. ΔV_{out} of the memristive crossbar read operation for different numbers of rows. More rows require higher sense amplifier resolution for the circuit. This is a disadvantage that was predicted in (5) and (8). The simulation shows that the main challenge in this type of crossbar is the quality of the sense amplifier. The number of columns is $N = 4$, $V_{read} = 1V$, R_{ref} is selected according to (10), $R_{wire} = 1.25\Omega$ and $C_{wire} = 0.01fF$. [Colour figure can be viewed at wileyonlinelibrary.com]

when increasing the number of rows and columns (for an $\frac{N}{2} \times N$ crossbar), the overall energy increases as determined in (14). Figure 14 shows that the noise margin, determined by ΔV_{out}, decreases with larger number of rows, while it is unaffected by the number of columns, as determined in (8). The figures present an excellent match between the simulation results and the analytic calculations in terms of energy, read latency, and noise margin.

The simulation parameters are as follows: ferroelectric memristors with $R_{on} = 150k\Omega$, $R_{off} = 45M\Omega$ [31], and a sense amplifier with settling time $T_{settling} = 150ps$, $C_{SA} = 5fF$, $R_{wire} = 1.25\Omega$ and $C_{wire} = 0.01fF$. All other parameters vary between simulations and are listed in the figure captions. Note that for Figures 10 and 13, V_{read} was chosen to be minimal (so that the output voltage is still distinguishable, as shown in (5) and (8)), that is, every data point has a different V_{read}, and the trends shown in these graphs represent the optimized configuration (minimal energy) for every crossbar size.

8. CONCLUSIONS

The row grounding technique along with voltage divider sense circuit load optimization allows the design of large crossbar arrays while maintaining sufficient output voltage noise margins. We find that increasing the number of columns linearly increases the energy of the crossbar as seen in Figure 11 and (14), with negligible effects on the energy per bit, read latency, and output voltage. In contrast, increasing the number of rows decreases the output voltage (thus degrading the noise margin and calling for the use of sense amplifiers with better sensitivity). In some cases, however, increasing the number of rows also diminishes the read latency, as deduced from (8) and (12), thus reducing energy as seen in Figure 12.

Although larger arrays with a fixed row-column ratio consume more energy, adding more rows without increasing the number of columns sometimes improves the read latency. This characteristic is fundamentally different from charge-based memories, such as static random-access memory and dynamic random-access memory, and gives motivation to use row grounding to enhance the performance of memristive memories.

The voltage divider readout scheme combined with the row grounding technique presented in this paper is one of several possible design methodologies for a memristive crossbar. In future work, we intend to investigate other techniques, such as the trans-impedance amplifier readout scheme [33], and compare them to row grounding.

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APPENDIX A: READ LATENCY CALCULATION OF AN *M*-BY-*N* CROSSBAR ARRAY

This appendix shows how we developed the expression in (12). Figure A.1 illustrates the method we used to determine the crossbar delay. The crossbar has been marked with four rectangles, $\tau_1 - \tau_4$, each determined separately using the Elmore delay formula presented in (11).

The calculation begins with the left-most side of the crossbar array, with the first node near V_{read}, using the Elmore delay formula,

$$\tau_{first} = R_{wire} \cdot C_{wire}.$$

The second node near V_{read} has a delay of

$$\tau_{second} = \tau_{first} + 2 \cdot R_{wire} \cdot C_{wire}.$$

The delay of the second node is composed of all the resistors in the path from the input voltage to the node. Using the same method until we reach the end of the row (rectangle τ_1), we obtain the expression

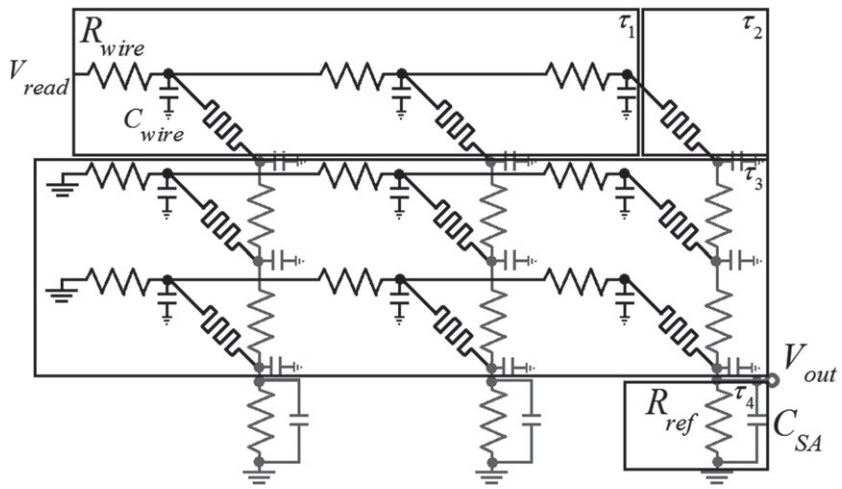

Figure A.1. 3-by-3 memristive crossbar with wire resistance and capacitance modeling. Each column is connected to a reference resistor R_{ref} and a sense amplifier with capacitance C_{SA}. In order to simplify the crossbar delay calculation, the crossbar has been marked with four rectangles, $\tau_1 - \tau_4$, calculated separately using the Elmore delay formula (12).

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for τ_1, which represents the row delay:

$$\tau_1 = \sum_{i=1}^{N} \left[C_i \cdot \sum_{k=1}^{i} R_k \right] = R_{wire} \cdot C_{wire} + 2 \cdot R_{wire} \cdot C_{wire} + \cdots + N \cdot R_{wire} \cdot C_{wire} = R_{wire} \cdot C_{wire}(1 + 2 + \cdots + N) = R_{wire} \cdot C_{wire} \cdot \frac{(N+1) \cdot N}{2}.$$

τ_2 represents the delay of the selected memristor and is calculated in a similar manner, where all the resistances in the path from the input to the node below the memristor are taken into account:

$$\tau_2 = C_{wire} \cdot (R_{on} + N \cdot R_{wire}).$$

τ_3 represents the column delay, and the first node in the column has a delay of

$$\tau_{first_{col}} = [(R_{on} + N \cdot R_{wire}) \parallel (R_{on} + N \cdot R_{wire})] \cdot C_{wire}.$$

This expression represents the two upper rows of the crossbar. Calculating the contribution of the first and second row to the time delay in parallel is justified using the same method shown in Figure 3 and calculated in (4), the resistances in the two rows contribute in parallel to the charge time of the node capacitance. The second node in the column has a delay of

$$\tau_{second_{col}} = \tau_{first_{col}} + [(R_{on} + N \cdot R_{wire}) \parallel (R_{on} + N \cdot R_{wire}) \parallel (R_{on} + N \cdot R_{wire})] \cdot C_{wire},$$

where the second addend represents the three upper rows of the crossbar. $M-1$ iterations of this formula (as the number of row capacitances in the τ_3 rectangle) result in

$$\tau_{col} = \sum_{i=1}^{M-1} \left[C_i \cdot \sum_{k=1}^{i} R_k \right] = (R_{on} + N \cdot R_{wire}) \cdot C_{wire} \cdot \sum_{i=2}^{M} \frac{1}{i}.$$

This can be approximated using a partial sum of harmonic series [41], which results in

$$\tau_3 = \tau_{col} = C_{wire} \cdot (R_{on} + N \cdot R_{wire}) \cdot \left(ln(M) + 0.577 + \frac{1}{2 \cdot M} - \frac{1}{12 \cdot M^2} - 1 \right).$$

Note that to simplify the calculation, we disregard a single wire resistance for each row in the calculation of τ_3. This is justified because $R_{wire} << (R_{on} + N \cdot R_{wire})$, as derived in (6). Moreover, the wire capacitances in the grounded crossbar rows are not taken into account in this calculation because the wires in each row are charged through all columns simultaneously. Thus, no additional delay is contributed by those capacitances. This assumption is confirmed by the simulation results.

τ_4 represents the delay of the sense circuit. It comprises the resistances in the path from the input to the sense amplifier node, where R_{eq} includes the resistance of the column memristor in parallel, as derived in (8).

$$\tau_4 = C_{SA} \cdot (R_{eq} \parallel ((M + N - 1) \cdot R_{wire} + R_{on})).$$

Summing τ_1 to τ_4 and multiplying it by 2.2 (a typical approximation for an equivalent RC circuit rise time from 10% to 90% of the final voltage) result in the cumulative delay of the memristor crossbar, as derived in (13).

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