

# A Lumped RF Model for Nanoscale Memristive Devices and Non-Volatile Single-Pole Double-Throw Switches

Nicolás Wainstein and Shahar Kvatinsky, *Member, IEEE*

**Abstract**—In this paper, a scalable lumped model that accurately predicts the steady-state high-frequency behavior of nanoscale RF memristive devices is presented. The model is described (a) analytically by a set of closed-form equations that determine the parameters based on the device physical structure, allowing for optimized circuit design and performance through structure modifications, and (b) numerically to fit the model parameters to experimental data, allowing for evaluation of the accuracy of the model. This model is, to the best of our knowledge, the first lumped RF memristor model that includes device parasitics obtained from empirical measurements reported in the literature. Results show that the model is reasonably accurate, with 9.6% and 13% relative RMS error for the ON-state magnitude and phase, respectively. Furthermore, we propose three topologies (series, shunt and series-shunt) of non-volatile single-pole double-throw switches using our lumped RF memristor model. The series and shunt topologies are single-voltage-controlled, while the series-shunt requires two control signals. Simulation results of these topologies exhibit low insertion loss and high isolation (below 0.25 dB and over 63 dB, respectively). The added non-volatility and nanoscale size will result in reduced power consumption and higher density devices.

**Index Terms**—Memristors, memristive devices, modeling, radio frequency, RFIC, SPDT switches, nanoscale devices, scattering parameters.

## I. INTRODUCTION

MINIATURIZATION and low-power consumption are compelling trends in wireless systems, as the Internet of Things (IoT) requires wireless connections in all sorts of devices and appliances. The challenge then is to ensure high performance while continuing the trend. The high throughput demand needs to be addressed with higher spectral efficiency (namely, using multiple-input multiple-output (MIMO) antennas [1]), spatial reuse (*i.e.*, using beamforming [2]), and more spectrum (*i.e.*, moving to higher frequencies). Furthermore, multi-frequency/multi-protocol RF systems (namely, reconfigurable architectures) are in high demand. These architectures

allow different protocols to be supported, reducing or eliminating the need for a separate RF chain for each band; they also enable blocks to be reused, and they radically reduce the area of wireless front-ends, while adding flexibility to the systems. There is thus a need for new technologies that can provide the required scalability, low-power consumption, high performance and reconfigurability to face the new challenges in communications.

The current solutions rely on transistor-based and micro-electromechanical systems (MEMS)-based switches. MEMS are superior to InGaAs and Si transistor-based switches in terms of energy consumption and RF transmission parameters. However, they are undermined by issues such as dielectric charging, low switching speed, contact interface degradation, and large area overhead [3]. Transistor-based switches provide fast switching but require a large area to achieve a low resistance in the ON state, which results in a large parasitic capacitance [4], [5].

Recently, memristive devices have emerged as promising candidates for RF switches [6]–[8], due to their achievable low insertion loss (IL), high isolation (IS) and high cutoff frequency. Memristive devices are two-terminal passive circuit elements with varying resistance (namely, memristance), which depends on a state variable (or a set of state variables). The state varies according to the history of the applied voltage or current stimuli, and is retained whenever the voltage or current is no longer applied [9], [10]. These devices can be used as switches with discrete states, as they exhibit nonlinear behavior with a high resistive state (HRS,  $R_{OFF}$ ) and a low resistive state (LRS,  $R_{ON}$ ). Switching from  $R_{OFF}$  to  $R_{ON}$  is called ‘set’, while the opposite switching is called ‘reset’. These devices have proven to be an attractive feature also for memory, logic, and neuromorphic applications due to their non-volatility, low switching time and energy, better scalability, small footprint, and CMOS integration compatibility [11].

The non-volatility of memristors implies that no bias voltage or current is required to maintain a particular state, hence reducing the energy consumption. Moreover, their small size can improve the density of transceiver chains in MIMO systems. In their physical realization, memristors are usually fabricated in the back-end-of-line (BEOL) of standard transistor process which can reduce the need for routing signals from the top metal layer to the transistor layer, hence reducing the RF power losses and possible area overhead. Memristors can also add tunable capabilities (among others) to passive devices that traditionally stand on the top metal layers (*e.g.*, MIM

N. Wainstein and S. Kvatinsky are with the Andrew and Erna Viterbi Faculty of Electrical Engineering, Technion – Israel Institute of Technology, Haifa 32000, Israel (e-mail: {nicolasw@campus},{shahar@ee}.technion.ac.il).

This research is partially supported by the Viterbi Fellowship at the Technion Computer Engineering Center and by the Intel Collaborative Research Center for Computational Intelligence.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Copyright (c) 2018 IEEE. Personal use of this material is permitted. However, permission to use this material for any other other purposes must be obtained from the IEEE by sending a request to [pubs-permissions@ieee.org](mailto:pubs-permissions@ieee.org).

capacitors, and spiral inductors).

Several physical and mathematical models have been developed to describe the switching dynamics of memristive devices [12]–[15]. However, precise and scalable lumped physical models that could describe the behavior of the device at high frequencies were lacking. In [16], we introduced a scalable lumped model that predicts with sufficient accuracy the high frequency behavior of RF memristive switches (RFMS) in a coplanar waveguide (CPW) transmission line. The model relies on the voltage threshold adaptive memristor (VTEAM) model [13] to predict the transient behavior (*i.e.*, describes the changes in the memristance) and introduces a structure-inspired lumped RLC circuit to describe its steady-state behavior at high frequency. The model is further divided into an analytic and a numerical model. The former is composed of a set of closed-form equations taken from previous works in RF modeling. The latter is a behavioral model that is used to fit experimental data, for this work, obtained from [6]. The use of the lumped model was demonstrated by designing and evaluating two novel topologies of non-volatile Single-Pole Double-Throw (SPDT) RF switches with a single bias voltage.

In this paper, the analytic and numerical models are extended and improved. We compare the proposed model with electromagnetic (EM) simulations performed in Advanced Design System (ADS) from Keysight Technologies [17]. We present the switching dynamics fitting to the VTEAM model, the fitting procedure and results. Moreover, transient simulations using the proposed model as part of the VTEAM model are presented. New design trade-offs and insights regarding how to optimize the device structure to obtain a desired performance are also presented. Furthermore, we propose a new topology of SPDT, the series-shunt, that enhances the performance without introducing a significant area overhead. The results of the previously presented topologies are extended to include the return loss (RL), and a comparison between the three topologies is added.

## II. RF MEMRISTIVE SWITCHES AND MODELS

### A. RF Memristive Switches

Most previously proposed RFMS can be characterized as electrochemical metallization (ECM) memristors [18], consisting of a pair of electrochemically asymmetric metal electrodes separated by a small-scale gap or an insulator. The switching mechanism is determined by the formation or rupture of a conductive filament between two electrodes owing to electrochemical reactions, ion migration, and Joule heating [19]. At LRS, a thin metal filament shortens the electrodes, while at HRS the filament disappears (or is reduced). An interesting property of these devices is the linear dependence of  $R_{ON}$  on the compliance current [6], [18]; the higher the compliance current, the lower the achieved  $R_{ON}$ .

Fig. 1 shows the device structure presented in [6], where Ag and Ti/Au/Ag electrodes (active and inert, respectively) are separated by a 35 nm air gap. The device is fabricated over a  $\text{SiO}_2$  surface in a high resistivity silicon substrate, in-line with a CPW transmission line. The reported device presents an IL of approximately 0.3 dB and an IS of over 30 dB at 40 GHz,

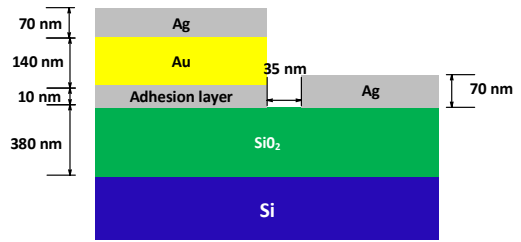


Fig. 1. Physical structure schematic of the RFMS proposed in [6]. Two metal electrodes (Ag and sandwiched Ti/Au/Ag respectively) separated by a 35 nm air gap in-line on a CPW.

and a typical cut-off frequency of 35 THz. The reported  $R_{ON}$  is 2.6  $\Omega$ ,  $R_{OFF}$  is in the order of 1 T $\Omega$  and the OFF-state capacitance,  $C_{OFF}$ , is on average 1.41 fF. The LRS and HRS are achieved by applying, respectively, 3 V and -0.4 V across the electrodes. The reported power handling capabilities of the switch this switch is 17 dBm, at which the device starts to self-switch. The authors claim that frequencies above 40 GHz could be achieved by canceling undesired substrate moding effects that perturb the performance of the switch, for example by integrating the device in a grounded CPW structure.

Nessel *et al.* have presented a 10  $\mu\text{m}$  gapless-type ECM RFMS with Ag and Ni electrodes (active and inert, respectively) [7]. Measurements from 1 to 6 GHz demonstrate an IL of less than 0.5 dB and an IS better than 30 dB. The voltage/current required to change the state of the device is nominally 1 V/10 mA (SET) and -1 V/10 mA (RESET). In [8], a Cu/ $\text{SiO}_2$ /Al ECM RFMS is presented. This switch has been characterized at 0.15 GHz, achieving an IL of 1.6 dB and an IS of 20 dB. Regardless of its lower performance when compared to the aforementioned RFMS, it stands out for its simple structure, and therefore its simpler fabrication process.

Another family of RFMS are phase change materials (PCM)-based switches. The switching mechanism in these devices relies on transitioning between the amorphous (insulating) and crystalline (conductive) states of a chalcogenide, which is accomplished by heating and cooling the PCM. In [20], [21], inline PCM RF switches are presented. These switches can achieve an IL of 0.15 dB and an IS of 15 dB at 18 GHz. The device requires a significantly larger area than ECM switches, the required programming voltages exceed 10 V, and for some compounds the device is required to be kept above a certain temperature to retain the LRS (*e.g.*, 67°C for  $\text{VO}_2$ ).

### B. RFMS Models

Models are indispensable tools in circuit design and simulation, as they simplify the understanding of the device and predict its behavior. Precise models allow accurate circuit designs, device optimization, and the fullest possible exploitation of the device characteristics. In both [6] and [8], the RFMS is modeled as a simple parallel RC circuit. A first order analysis of the physical parameters is described in [6], where the LRS resistance and the gap capacitance ( $R_{ON}$  and  $C_{OFF}$ , respectively) are theoretically determined. Though the models are sufficiently accurate to describe the IL and IS of the device,

they do not fully describe its S-parameters (*i.e.*, its steady-state high-frequency electrical behavior). Furthermore, neither the skin effect of the conductors nor the parasitic capacitance [22] at the electrodes are considered in these models. These effects will be dominant at high frequencies, and will determinate the RFMS performance and influence the matching network design.

An RF memristor model that predicts the maximum switching frequency in which a memristive memory cell can be operated is proposed in [23]. While this model considers further high-frequency phenomena, it is still a transient (time-dependent) model, thus not intended to describe the S-parameters of the memristor. In [24], a finite-difference time-domain implementation (FDTD) of the memristor using the non-linear ion drift model [25] is proposed. This model allows an electromagnetic-wave analysis of the memristor, yet it lacks the capacitive and inductive parasitics present in real devices.

### C. VTEAM Model

The VTEAM model [13] accurately describes voltage-controlled memristive devices and relies on a voltage threshold parameter. The derivative of the internal state variable  $x$  is

$$\frac{dx}{dt} = \begin{cases} k_{on} \left( \frac{v(t)}{v_{on}} - 1 \right)^{\alpha_{on}} f_{on}(x), & v < v_{on} < 0, \\ 0, & v_{on} < v < v_{off}, \\ k_{off} \left( \frac{v(t)}{v_{off}} - 1 \right)^{\alpha_{off}} f_{off}(x), & 0 < v_{off} < v, \end{cases} \quad (1)$$

where  $k_{on}$ ,  $k_{off}$ ,  $\alpha_{on}$ , and  $\alpha_{off}$  are fitting parameters. Voltages  $v_{on}$  and  $v_{off}$  are the ON and OFF threshold voltages, respectively. Functions  $f_{on}(x)$  and  $f_{off}(x)$  describe the relation between the derivative of the state variable and the state variable  $x$ . These functions are window functions which bound the internal state variable between  $[x_{on}, x_{off}]$ . The model is modified to support the aforementioned relationship between the compliance current and  $R_{ON}$ ; hence the compliance current must be provided to determine  $R_{ON}$ . The voltage-current relationship is

$$i(t) = \left[ R_{ON} + \frac{R_{OFF} - R_{ON}}{x_{off} - x_{on}} (x - x_{on}) \right]^{-1} v(t). \quad (2)$$

To be consistent with the polarity convention of this model, the polarity of  $V_{SET}$  and  $V_{RESET}$ , the set and reset voltages, respectively, is swapped from the convention in [6]–[8], [18]; hence  $V_{RESET}$  is positive, while  $V_{SET}$  is negative.

## III. PROPOSED RFMS LUMPED MODEL

In this section, the proposed lumped model is described. For the analytic model, we surveyed the literature for closed-form expressions that accurately describe the elements of the model from the dimensions of the structure. The numerical model is a behavioral implementation which can be fitted from empirical data. Finally, the fitting procedure to the VTEAM model is described.

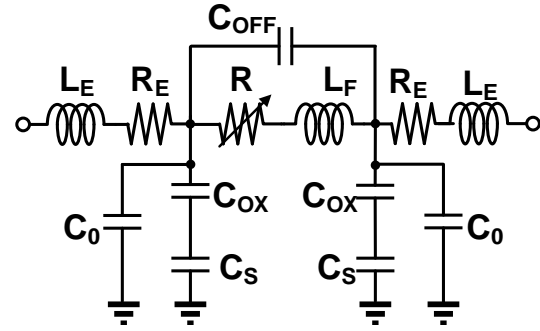


Fig. 2. Extended from the proposed model in [16]. The resistance of the electrodes is now considered.

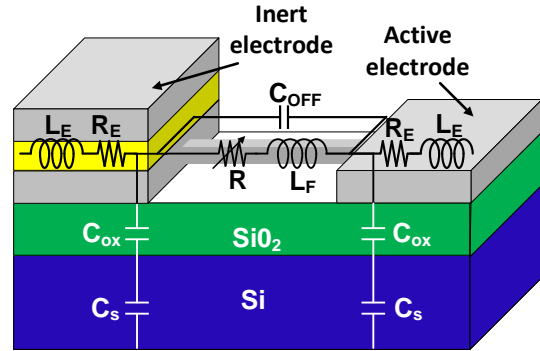


Fig. 3. 3D cross-section of the device presented in [6] with the lumped elements overlapped. Capacitor  $C_0$ , coupling capacitor between signal line and ground plane, is not shown here.

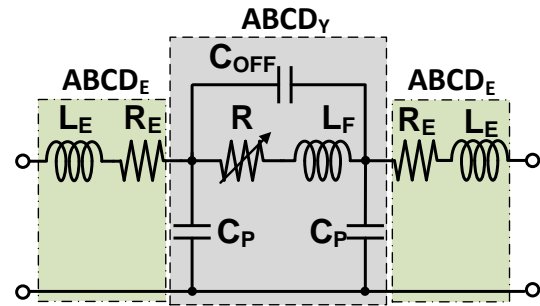


Fig. 4. The lumped circuit is divided into three  $ABCD$  matrices.  $ABCD_Y$  (in gray) is the transformation into  $ABCD$ -parameters from a  $Y$ -equivalent  $\pi$  two-port network.  $ABCD_E$  describes the impedance of the electrodes,  $R_E + j\omega L_E$ .

### A. Proposed RFMS Model Description

Based on an examination of the memristive device structure presented in [6], we propose a novel and more accurate model, shown in Fig. 2. As in [6],  $R$  and  $C_{OFF}$ , represent the memristance and the gap capacitance (*i.e.*, the capacitive coupling effect between the electrodes), respectively. Additional capacitors are added to represent the  $\text{SiO}_2$  parasitic capacitance,  $C_{ox}$ , the Si substrate capacitance,  $C_s$ , and the fringe capacitance between the signal line and ground planes,  $C_0$ . The inductance of the filament and the electrodes are also considered and are, respectively,  $L_F$  and  $L_E$ . The resistance  $R_E$  describes the losses in the electrodes. A 3D cross-section

of the device with the lumped elements of the proposed model is shown in Fig. 3.

The model is consistent with previous work in CPW and RF lumped device modeling [26]–[28]. Particularly, in the steady-state at high frequency, the device is considered as a gap discontinuity in the CPW at HRS and as a high impedance short-line section at LRS. The switching dynamics of the memristance are based on the VTEAM model. The assumptions in this model are (a) lossless substrate (*i.e.*, high resistivity silicon), and (b) identical conductor electrodes (*i.e.*, equal  $L_E$  and  $R_E$  in both electrodes).

### B. Analytic Model

The analytic model provides a set of closed-form equations to determine the lumped elements in the proposed model directly from the dimensional parameters of the RFMS structure proposed in [6] in a steady-state high frequency regime. The steady-state ON-state resistance of the filament, along with the resistance of the electrodes, account for the skin depth of a conductor with finite thickness and are

$$R_{ON} = \frac{\rho_{fil} l_{gap}}{W_{fil} \delta_{Ag} (1 - e^{-t_{fil}/\delta_{Ag}})}, \quad (3)$$

$$R_E = \frac{\rho_E l_E}{W_E \delta_{Au} (1 - e^{-t_E/\delta_{Au}})}, \quad (4)$$

where  $\rho_{fil}$ ,  $l_{gap}$ ,  $W_{fil}$ ,  $t_{fil}$  are, respectively, the metal resistivity at DC, length, width and height of the filament. Similarly,  $\rho_E$ ,  $l_E$ ,  $W_E$ ,  $t_E$  are the resistivity, length, width and height of each electrode, respectively. The skin depth,  $\delta$ , depends on the frequency and the resistivity of the materials (Ag and Au, respectively). The width of the filament depends on the compliance current, *i.e.*, the higher the compliance current, the wider the filament, and thus a lower  $R_{ON}$  is achieved.

The between-electrodes (gap) capacitance is modeled as

$$C_{OFF} = \frac{\varepsilon_0 \varepsilon_{eff} A_{BE}}{l_{gap}} k, \quad k \in [1.3, 1.6], \quad (5)$$

where  $A_{BE}$  is the lateral section of the electrodes and  $k$  is a dimensionless constant that accounts for the fringe capacitance, which is between 30% to 60% of the parallel plate capacitance [3]. The effective relative permittivity,  $\varepsilon_{eff}$ , is calculated as in [28]. The SiO<sub>2</sub> parasitic capacitor is determined by the SiO<sub>2</sub> height,  $t_{ox}$ , the width of the electrode,  $W_E$ , and the SiO<sub>2</sub> relative permittivity,  $\varepsilon_{ox}$ , and is

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}} (W_E + 1.5 t_{ox}). \quad (6)$$

The silicon substrate capacitance,  $C_s$ , and the fringe capacitance,  $C_0$ , are

$$C_s = 2(\varepsilon_{Si} - 1)\varepsilon_0 F_{Si}, \quad C_0 = 4\varepsilon_0 F_0, \quad (7)$$

where  $\varepsilon_{Si}$  is the silicon relative permittivity,  $F_{Si}$  is the silicon geometry factor, and  $F_0$  is the air geometry factor at the electrodes. The filament and electrode inductances are

$$L_F = \frac{\mu_0}{4F_{fil}}, \quad L_E = \frac{\mu_0}{4F_{0E}}, \quad (8)$$

where  $F_{fil}$  and  $F_{0E}$  are, respectively, the air geometry factor at the filament and the electrodes.

### C. Numerical Model

The numerical model is a behavioral implementation to fit the lumped parameters from experimental data (here, from [6]). As shown in Fig. 4, the proposed model can be described as three cascaded two-port network  $ABCD$ -transmission matrices. Matrix  $ABCD_E$  is the two-port matrix that describes the RL series circuit corresponding to the electrodes. The middle section of the model, highlighted in gray in Fig. 4, can be analyzed as a Y-equivalent  $\pi$  two-port network, where

$$Y_{12} = - \left( \frac{1}{R(f) + j\omega L_F} + j\omega C_{OFF} \right), \quad (9)$$

$$Y_{11} + Y_{12} = Y_{22} + Y_{12} = j\omega C_p, \quad (10)$$

where  $C_p$  is the equivalent capacitor of  $C_s$ ,  $C_{ox}$  and  $C_0$  as shown in Fig. 4. Since the resistance depends on the frequency as predicted by the skin effect, in this work we added this dependency and defined  $R(f)$  as  $\overline{R_{ON}} + k\sqrt{f}$ , where  $\overline{R_{ON}}$  and  $k$  are fitting parameters, being  $k$  the parameter associated to the additional resistance due to the skin effect. The Y-equivalent  $\Pi$  is transformed to  $ABCD$ -parameters to define  $ABCD_Y$ . The total  $ABCD$  matrix,  $ABCD_{Total}$ , is the product of the three matrices.

The fitting flow is described in Fig. 5. A theoretical  $ABCD$  matrix is built using seed parameters and then transformed to S-parameters. Initial fitting is done using the Simulated Annealing [29] algorithm to search for the minimum relative root mean squared error (RMSE) between the experimental and modeled S-parameters. Then, using the obtained  $ABCD_E$  matrix,  $ABCD_Y$  is determined as

$$ABCD_Y = ABCD_E^{-1} \cdot ABCD_{Total} \cdot ABCD_E^{-1}, \quad (11)$$

and is then transformed to a Y-matrix. Parameters  $C_p$ ,  $L_F$  and  $R$  can be extracted by fitting (9) and (10). Capacitor  $C_{OFF}$  is determined from the OFF-state (HRS) S-parameters, where  $Y_{12} \simeq -j\omega C_{OFF}$ . Several iterations can be done to achieve more accurate results. The extracted parameters from the fitting procedure are listed in Table I.

### D. Fitting the VTEAM Model

As mentioned, the VTEAM model is used to describe the switching dynamics of the RFMS. Owing to the generality of the VTEAM model, it can be fit to diverse memristive models and experimental data. Since the speed of the device has not been characterized, results from [30] indicate that the electrodeposition rate of silver is approximately 1 nm/ns. Hence, for this device a switching time of 35 ns is assumed as a lower bound since the air-gap is 35 nm wide. To fit the I-V curve to VTEAM, the Gradient Descent algorithm [31] is used to minimize the relative RMSE. An ideal window is used in the fitting procedure. Results for the fitting procedure are presented in section IV-D.

## IV. MODEL EVALUATION

In this section, the proposed model is evaluated First, the proposed lumped model is compared against the RC model [6] and then by examining the extracted parameters from the

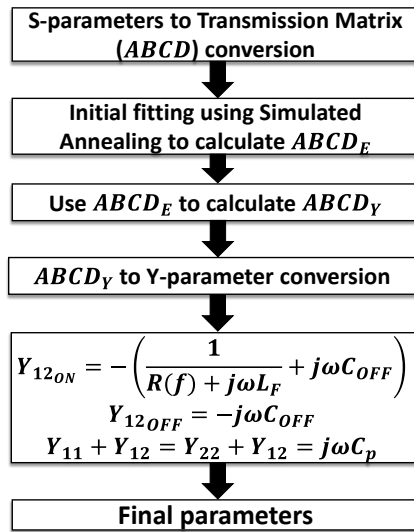


Fig. 5. Fitting flow procedure for numerical model. The procedure can be repeated several times to increase the accuracy.

TABLE I  
COMPARISON OF DIFFERENT MODELS

Parameter	Numerical Model		Analytic Model
	RC Model [6]	This work	This work
$R_{ON}$ <sup>1</sup>	2.8 $\Omega$	2.2 $\Omega$	2.16 $\Omega$
$C_{OFF}$	1.145 fF	1.145 fF	1.168 fF
$C_p$	-	3.08 fF	1.15 fF
$L_F$	-	77 fH	52 fH
$L_E$	-	3.7 pH	3.1 pH
$R_E$	-	0.2 $\Omega$	0.2 $\Omega$
$k$	-	1.4 $\mu\Omega/\sqrt{Hz}$	-

<sup>1</sup>  $R_{ON}$  is here the average resistance along the whole band

fitting procedure with respect to the analytic model determined by expressions (3)-(8). The former evaluation demonstrates the improvement in the accuracy of the device model. The latter provides an estimation of the proximity between the analytic model (namely, the physics-based model) parameters and the numerical model (namely, the extracted parameters). Furthermore, the model is compared to EM simulations obtained from a momentum 3-D planar electromagnetic simulator. Note that as the reference planes used for de-embedding the measurements in [6] were placed 15  $\mu m$  one from the other, the extracted parameters in the numerical model and in the analytic model, as well as the EM simulations include sections of the CPW feed-lines from the de-embedding process. Finally, the results of the VTEAM model fitting for the switching dynamics are presented.

#### A. RC Model vs. Proposed Model

Following the fitting procedure presented in section III-C, the model parameters are extracted. The result of the fitting procedure for the RC model [6] and our model versus experimental results for ON and OFF states are shown in Fig. 6 and Fig. 7, respectively. Although the RC model exhibits a

good match with  $S_{21}$  magnitude, it can be observed that our proposed model improves the accuracy of the S-parameters, particularly of the phase (Fig. 6(b) and (d)), which is crucial for phase-sensitive applications and for designing matching networks. The phase shift becomes even more significant when extrapolating to higher frequencies, as the devices become more capacitive, due to the increasing influence of the capacitive coupling to the substrate.

The fitting parameters for both models are listed in Table I. The RMS error for the S-parameters is defined as

$$RMSE = \sqrt{\frac{1}{N} \left( \frac{\sum_{k=1}^N \left( S_{ij_{model}}^{(k)} - S_{ij_{meas}}^{(k)} \right)^2}{\bar{S}_{ij_{meas}}^2} \right)}, \quad (12)$$

where  $N$  is the number of samples,  $S_{ij_{model}}^{(k)}$  is the  $k$ -th sample of the S-parameters obtained from the model,  $S_{ij_{meas}}^{(k)}$  is the  $k$ -th sample the measured S-parameters, and  $\bar{S}_{ij_{meas}}$  is the Euclidean norm of the measured S-parameter. The overall improvement with respect to [6] in the relative RMS error are 32.5% and 87% for the ON state magnitude and phase, respectively. The improvement in the OFF-state phase RMS error is 33%. The lower accuracy is due to a significant error in the  $S_{21}$  phase, shown in Fig. 7(d), which is lower than the predicted 90°. The RC model is sufficiently accurate for the OFF-state  $S_{21}$  magnitude, hence no significant improvement is observed. An improvement of almost 10% in RMS error from our previous work [16] for the ON-state magnitude is observed. The improvement is due to the added resistance of the electrodes,  $R_E$ , together with the added fitting parameter  $k$ .

#### B. Analytic Model vs. Numerical Model

The parameters of the analytic model (*i.e.*, expressions (3)-(8)) and the numerical model are listed in Table I. The calculated parameters of the analytic model are quite close to those extracted by the numerical model. This confirms that the physical parameters predict with significant accuracy the high-frequency behavior of the RFMS. It worth noting that the parasitic capacitance,  $C_p$ , and the impedance of the electrodes,  $j\omega L_E + R_E$ , include part of the CPW losses, since the reference planes used for de-embedding the measurements in [6] were placed 15  $\mu m$  one from the other. In the physical structure, the reference plane includes part of the CPW signal line, which is wider than the electrodes of the memristive switch. This step change [28] can be modeled as a shunt capacitor [32], which increases  $C_p$  and explains the difference between the calculated parameter and the extracted parameter. Furthermore, it can be inferred that the performance of the intrinsic switch is even better than what is implied by measurements. Additional improvements in the model should add an analytic expression of the fringe capacitance at the gap. To validate this model, further tests should be performed with different data sets and different devices, varying the size of the electrodes, the gap and the CPW structure.

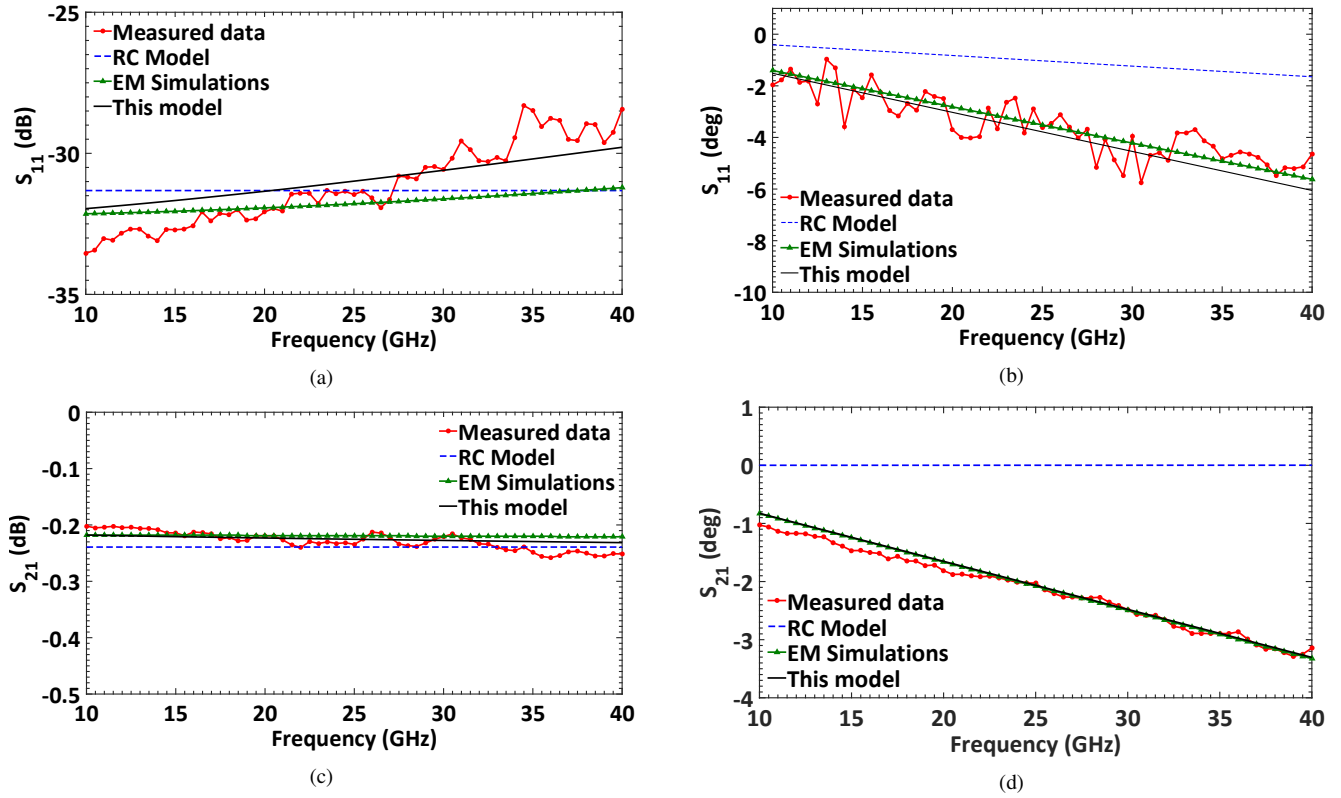


Fig. 6. S-parameter simulation results for ON state (LRS) as determined by the proposed model (black) and the RC model in [6] (blue dashed line) vs. EM simulations (green) and experimental data (red line). (a)  $S_{11_{ON}}$  magnitude, (b)  $S_{11_{ON}}$  phase, (c)  $S_{21_{ON}}$  magnitude, (d)  $S_{21_{ON}}$  phase.

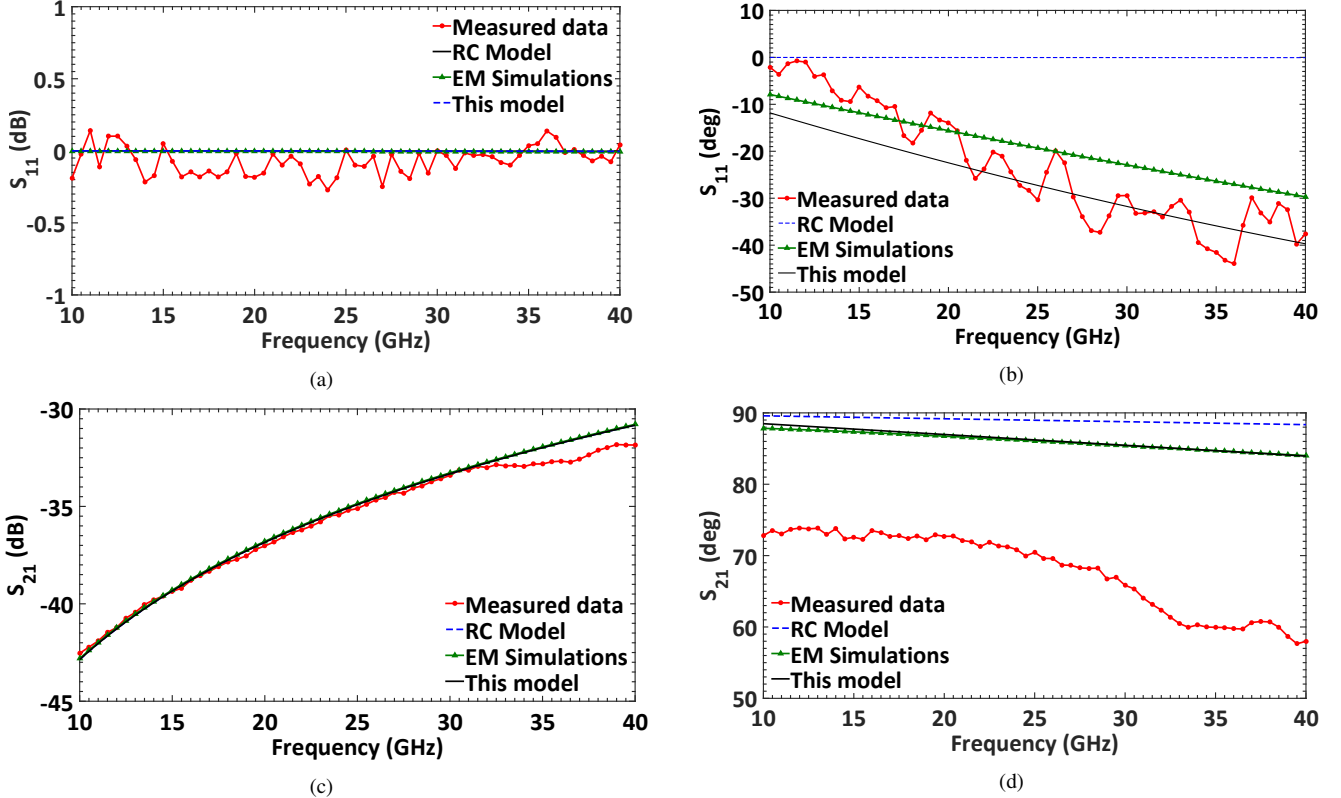


Fig. 7. S-parameter simulation results for OFF state (HRS) as determined by the proposed model (black) and the RC model in [6] (blue dashed line) vs. EM simulations (green) and experimental data (red line). (a)  $S_{11_{OFF}}$  magnitude, (b)  $S_{11_{OFF}}$  phase, (c)  $S_{21_{OFF}}$  magnitude, (d)  $S_{21_{OFF}}$  phase.



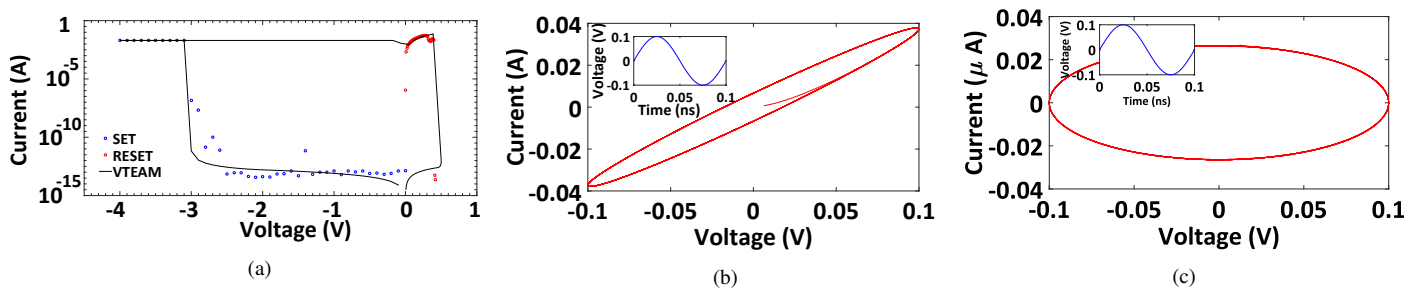


Fig. 8. (a)  $i$ - $v$  curve of experimental results [6] fitted to the VTEAM model. Experimental data for SET (blue circles), RESET (red circles) and fitted VTEAM model (black line). The polarity follows the convention in [13]. (b-c) Simulated transient  $i$ - $v$  characteristics of the RFMS for a sinusoidal input (inset) with  $f_o = 10$  GHz, (b) RFMS in HRS (c) RFMS in LRS.

### C. Numerical Model vs. EM Simulations

EM simulations were performed in ADS, using the dimensions of the CPW detailed in the supplementary material of [6]. To be consistent with the measurements, the reference planes used for de-embedding the results were placed  $15 \mu m$  one from the other. As in [6], for the ON-state simulations, a small rectangular silver filament was used to short the gap between the electrodes. It can be observed in Fig. 6 and Fig. 7, there is a good agreement between the analytic model and the EM simulations. The overall RMS error are 6.3% and 1.7% for ON and OFF states respectively. The discrepancy in the ON state comes from  $S_{11}$  amplitude which was fitted to the measurements. Furthermore, it can be seen in Fig. 7(c) that our model successfully describes the high-frequency characteristics without moding effects of the substrate that are present at the OFF state beyond 35 GHz. In Fig. 7(d), it is observed that the EM simulations also show a large difference with the measured  $S_{21}$  phase, thus this difference can be attributed to the de-embedding using a Thru-Reflect-Line (TRL) procedure which is different for the de-embedding process done in the EM simulations. In future work we intend to fabricate and measure different devices to further improve the model.

### D. Fitting the VTEAM Model

Results of fitting the VTEAM model to the experimental data are shown in Fig. 8(a). The obtained relative RMS error is below 1.53%. The resulting parameters are listed in Table II. It is worth noting that the compliance current in these measurements was  $20 mA$ , which leads to an  $R_{ON}$  of  $5.4 \Omega$ . With the obtained results, transient simulations can be performed. A high-frequency signal is applied when the device is in LRS (Fig. 8(b)) and an RC Lissajous plot is observed. When the device is HRS, the circuit responds as a capacitor (Fig. 8(c)). These results demonstrate that physical memristors at high frequency behave not as a linear resistor as theoretically predicted in [9], but rather as an RC circuit. Furthermore, when the memristor is at HRS, the capacitor is dominant.

## V. MEMRISTIVE RF SPDT SWITCHES

Single-Pole Double-Throw (SPDT) switches are basic elements of any modern RF system. These switches fulfill

TABLE II  
FITTING PARAMETERS OF THE VTEAM MODEL TO EXPERIMENTAL DATA

VTEAM OFF Parameter	Value	VTEAM ON Parameter	Value
$\alpha_{off}$	5	$\alpha_{on}$	0.5
$v_{off}$	0.4 V	$v_{on}$	-3 V
$R_{OFF}$	30 T $\Omega$	$R_{ON}$	5.4 $\Omega$
$k_{off}$	$10^{-5} m/s$	$k_{on}$	-10 m/s
$x_{off}$	0 nm	$x_{on}$	35 nm
I-V	Linear		

important functions in many RF applications, such as controlling the RF signal flow and providing multiple access to shared resources *e.g.*, antennas, phase shifters, and amplifiers [33]. These devices must provide a low ON resistance while conducting and a low OFF capacitance in the nonconducting state, to obtain a low IL and a high IS, respectively. This feature should be preserved over a broad frequency range.

PIN diodes have been the traditional block in RF switches owing to their low  $R_{ON}$  and  $C_{OFF}$ . However, a bias current is needed to maintain the state, thus incurring in a high static power consumption, which remains as a severe limitation. RF MEMS emerged as high-performance switches but still suffer, as mentioned, from contact degradation (due to their moving parts), high actuation voltages, dielectric charging, and slow switching time. Transistor-based switches provide high integration and fast switching. Nevertheless, state-of-the-art transistor-based SPDTs require large area to achieve sufficiently low  $R_{ON}$ , which results in high parasitic capacitance that must be cancelled using either inductors or stubs, hence incurring in a significant area overhead [4], [5], [34].

Nanoscale RFMSs exhibit high-performance characteristics, small size and non-volatility, which makes them an excellent candidate building block in high-performance, low power SPDT switches. With the proposed model, more accurate simulations can be achieved, making it possible to design and test RF SPDT switches and other RF applications. In this section, we propose three different RFMS SPDT topologies, shown in Fig. 9. The series and shunt make use of a single control-voltage (*i.e.*, a single bias signal) to simultaneously toggle the two output branches between LRS and HRS, while the series-shunt topology requires an extra control signal.

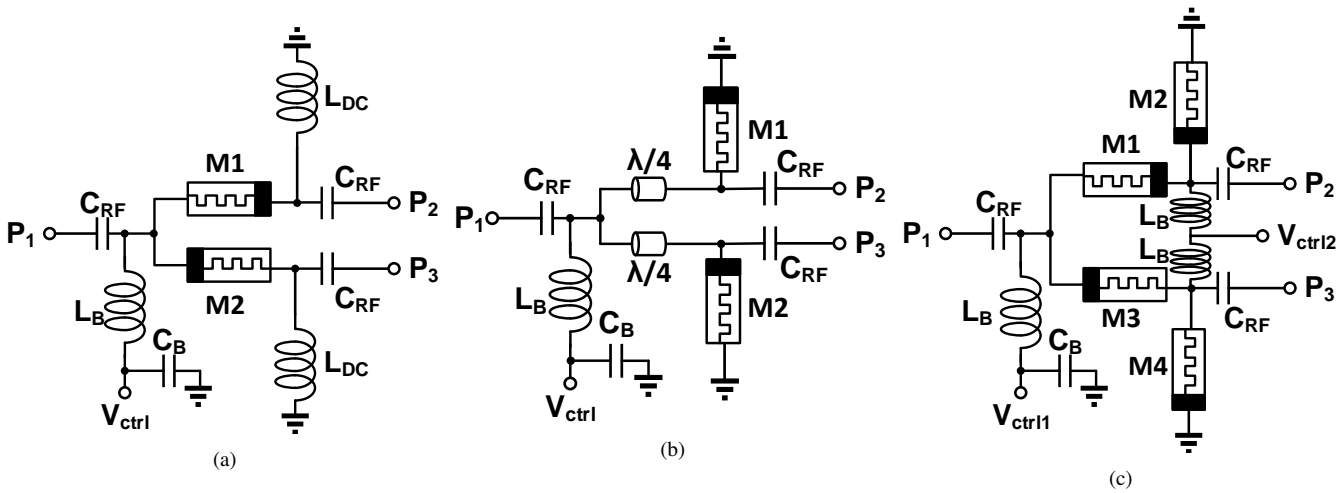


Fig. 9. Schematics of the proposed (a) series, (b) shunt, and (c) series-shunt RFMS SPDT topologies. Note that the CPW sections are not included in these schematics. Capacitors  $C_B$  and inductors  $L_B$  provide DC feeding and RF blocking. Capacitors  $C_{RF}$  are used for AC coupling. Inductors  $L_{DC}$  in (a) provide a DC reference to the memristors. In (b),  $\lambda/4$  is the quarter-wavelength transformer.

### A. Switch Design Trade-offs

The main trade-off in RF switch design when using FET and diodes is between their ON-state resistance and OFF-state capacitance. To achieve a low  $R_{ON}$  and thus improve the IL, a wide device is required. However, this degrades the IS as  $C_{OFF}$  increases, *e.g.*, in the case of FETs this capacitance is the drain-source capacitance,  $C_{ds}$ , which depends on the width of the diffusion region. As mentioned, inductors can be used to resonate this capacitance. However, due to the parasitic capacitance of physical inductors and their finite quality factor, this solution would be far from ideal.

A similar trade-off exists in RFMS, but here if the gap is reduced, a lower  $R_{ON}$  can be achieved, improving the IL, as the length in (3) decreases. Conversely,  $C_{OFF}$  increases, hence degrading the IS. A reduction in the switching time and the switching energy is also expected as the gap is reduced [35]. To further reduce  $C_{OFF}$ , and increase the IS, the electrodes section can be reduced. For instance, if it is reduced by two, then two memristors can be connected in parallel and achieve, up to parasitics, the same  $C_{OFF}$  and half  $R_{ON}$  as the starting device. Since the switching mechanism in ECM is exponentially dependent on the electric field [18], [36] the switching would not be affected by the parallel connection. However, smaller electrodes are prone to breakdown owing to large compliance currents required to achieve a low  $R_{ON}$ .

Another trade-off in RFMS exists between the switching energy and  $R_{ON}$ . As mentioned, the LRS is inversely proportional to the compliance current. Thus, if lower  $R_{ON}$  is desired, the compliance current must be increased. However, the switching energy will increase, which can also decrease the device endurance [37]. Furthermore, the minimum achievable  $R_{ON}$  is physically limited by the maximum current density supported by the electrodes, since it will limit the maximum possible compliance current during SET.

For the purpose of this paper, each memristive switch is assumed to have the extracted parameters in Table I. In this paper, the switch design is focused on achieving broadband

matching, *i.e.*, low RL, high IS and low IL, while utilizing a single overall control voltage. The topologies are simulated in Advanced Design System (ADS) from Keysight using the aforementioned model and CPW sections as in [6] (not shown in Fig. 9). Capacitors  $C_B$  and inductors  $L_B$  are considered ideal, as they could be part of a bias tee. Capacitors  $C_{RF}$  provide RF feeding and DC blocking. The elements in the circuit are interconnected with CPW sections (not shown in the schematic). Note that capacitors  $C_{RF}$  are not required if only RF input signals are guaranteed at ports  $P_{1-3}$  (*i.e.*, there is AC coupling at the ports). For simulation purposes  $C_{RF}$  are set to 10 pF. CPW transmission lines allow us to implement both series and shunt branches without using hot vias, which facilitates a more accurate design. We assume that no self-switching occurs at the band of interest [6] and we also assume cold-switching (*i.e.*, switching is done while no RF signal is applied).

### B. Series

The proposed series topology schematic is shown in Fig. 9(a), where a single RFMS per port is used (M1 and M2), and a single bias signal,  $V_{ctrl}$ , controls their state. Inductors  $L_{DC}$  have an inductance of 10 nH and a quality-factor of 21. They act as RF chokes and provide a DC reference for the memristors, thus avoiding floating nodes at DC. The circuit works as follows: when  $V_{ctrl} = 3$  V, M2 switches to LRS and M1 to HRS (observe the opposite connection); hence, it provides a conductive path for the RF signal from port P1 to port P3, while port P2 is isolated. Reciprocal analysis is done when  $V_{ctrl} = -3$  V. As the RESET mechanism is faster than the SET, particular care must be taken when designing the power supply to provide a defined compliance current to protect the RFMS. A possible implementation of the compliance current is to use a transmission gate (PMOS and NMOS transistors in parallel) that will provide a constant resistance to maintain the current below the desired value.

Simulation results are shown in Fig. 10(a). The obtained IS is over 36 dB and the IL is below 0.26 dB at the designed band.



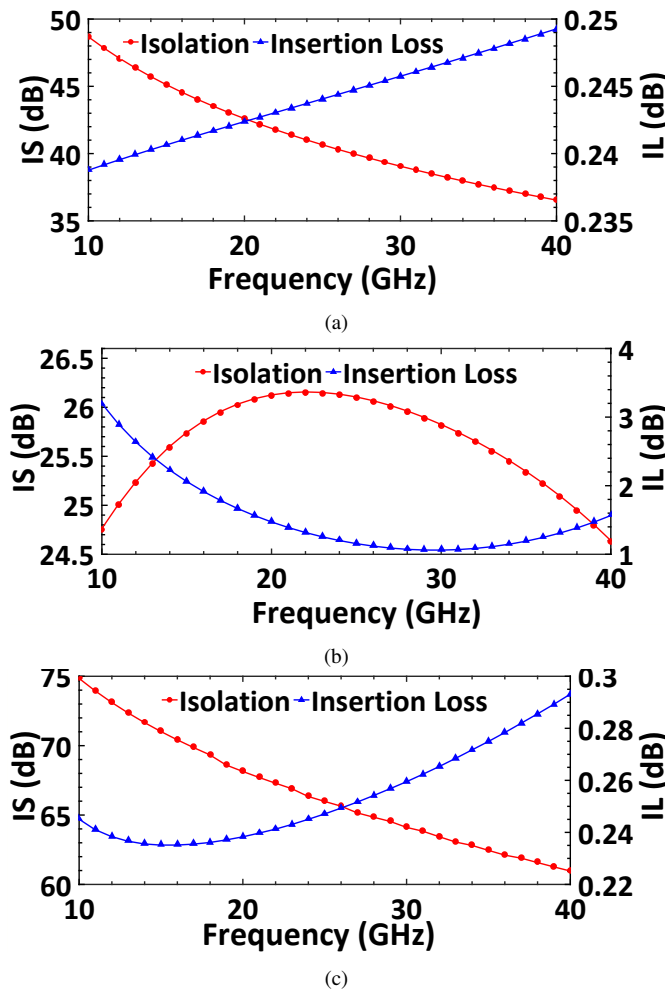


Fig. 10. Simulation results of IS (red) and IL (blue) of the proposed (a) series, (b) shunt, and (c) series-shunt SPDT topologies.

It presents a broadband performance over the desired spectrum and the expected 6 dB improvement in IS as compared to the single-pole single-throw (SPST) topology (*i.e.*, one input and one output with a single memristive switch). The RL is over 22 dB in the desired band, hence providing broadband matching.

### C. Shunt

The shunt topology is shown in Fig. 9(b). The RFMS M1 and M2 have one terminal grounded. As in the series topology, when  $V_{ctrl} = 3V$ , M2 switches to LRS and M1 switches to HRS, and vice versa for  $V_{ctrl} = -3V$ . The memristors provide a low resistive path to ground on LRS. This configuration makes use of the quarter-wavelength ( $\lambda/4$ ) transmission line (designed for 30 GHz) to transform the short-circuit (whenever the memristor is at LRS) into a high-impedance path, thus isolating the desired branch. When the memristor is at HRS there is a direct RF path between ports in the branch.

Simulation results for the shunt topology are shown in Fig. 10(b). The narrow-band characteristic provides an IL of 1 dB, an IS of 26 dB and an RL of 32 dB at 30 GHz. Its performance is remarkably lower than the series SPDT due to the lossy  $\lambda/4$  transformer. Moreover, the device becomes narrow-band and provides a lower IS than the series counterpart owing to  $C_{OFF}$

and  $C_p$ , which provide a low-impedance path to ground that considerably reduces the IS of the switch at higher frequencies. The IS can be improved by resonating this capacitance with an inductance. However, as the RF path does not pass through the memristor, higher power handling is also expected.

### D. Series-Shunt

To further increase the IS, we propose the series-shunt topology, illustrated in Fig. 9(c). This topology includes two RFMS per branch, connected with opposite polarity; hence when the series RFMS conducts (M1 or M3), the shunt RFMS (M2 or M4) is OFF, providing a conducting path for the RF signal. Conversely, when the series RFMS is OFF, the shunt RFMS is ON, thus increasing the IS (*i.e.*, there is high series impedance, and low impedance path to ground). Two control signals are required to program this topology,  $V_{ctrl1}$  and  $V_{ctrl2}$ . To program the series connected memristors  $M_1$  and  $M_3$ ,  $V_{ctrl1} = \pm 3V$  is applied while connecting  $V_{ctrl2}$  to ground. Similarly, to program the shunt memristors  $M_2$  and  $M_4$ ,  $V_{ctrl1} = V_{ctrl2} = \pm 3V$ .

Simulation results are shown in Fig. 10(c). An IL similar to that of the series topology is observed because, when a branch is conducting, the RF path goes through the series RFMS and the shunt RFMS is in HRS. Furthermore, the IS is increased by almost 25 dB. The obtained RL is over 22 dB. The drawbacks of this topology are the extra switching energy required to switch the added RFMS in each branch, the slight area overhead due to the added memristors, and the complexity and parasitics added due to the extra control signal  $V_{ctrl2}$ .

### E. Transient Simulations

As mentioned, the switching speed is an estimation based on the typical switching speed of ECM memristive devices. Transient simulations of the series and shunt topologies are shown in Fig. 11(a-b). Note that the SET process is sensitive to the parasitic resistance of the surroundings (*i.e.*, CPW sections, inductors) since the LRS is in the same order of magnitude. Thus, some of the voltage drop on the memristive device will be lower than expected, increasing the switching time. From Fig. 11(a-b), it can be observed that the shunt SPDT sets faster than the series being 77.5 ns and 119.3 ns, respectively. This is explained by the fact that the  $\lambda/4$  introduces less parasitic resistance than the RF choke inductors. RESET is less affected by the parasitic resistance and occurs at 44 ns for both cases.

In the series-shunt topology, the series memristors see the same parasitic resistance than that of the series topology, thus SET and RESET times are, as for the series SPDT, 119.3 ns and 44 ns respectively. The shunt memristors are similarly connected than in the shunt topology, but without a  $\lambda/4$ , thus the SET is slightly faster (75.6 ns), while RESET requires 44 ns as in the shunt topology.

### F. Comparison between Topologies

The series topology provides the better performance when a single RFMS per branch is used. The area required, if a fully integrated SPDT is considered, is larger for the shunt

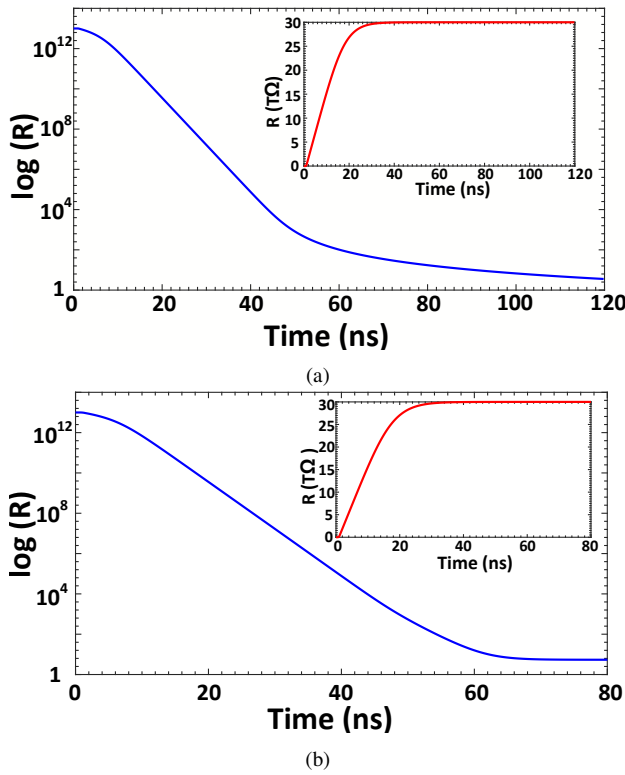


Fig. 11. Transient simulation results of SET (blue) and RESET (red in insets) of the proposed (a) series, and (b) shunt.

topology owing to the  $\lambda/4$  transformer. Furthermore, due to the latter, the shunt topology incurs in a narrow-band operation. The series-shunt topology significantly improves the IS while maintaining a low IL. The area required is slightly increased due to the added memristors. Hence, using two RFMS per branch in a series-shunt configuration improves the RF performance at the cost of a small area overhead.

Packaging introduces losses and may reduce the IS, particularly in the series-shunt topology due to the additional parasitic capacitance between the input and output ports. Thus, packaging needs to be carefully designed to preserve the integrity of the performance. For instance, in [38] a perfect magnetic conductor (PMC)-based packaging technique has been used to improve the isolation performance, allowing to reach isolations beyond 80 dB. The power handling capability is similar for all topologies since it is limited by the ON state, which may self-switch with input powers of over 17 dBm. Table III summarizes the comparison of the switch parameters.

## VI. CONCLUSIONS

An RF lumped model for memristive devices is described in this paper. The model describes and accounts for different physical phenomena in the device structure, by means of an analytic and numerical model. The analytic model allows the design and optimization of RFMS, while the numerical model serves as a fitting tool to simplify the analysis and the design of larger and more complex circuits. Fitting results to experimental data yields an improvement of 32.5% and 87% in relative RMS error for the ON-state magnitude and phase, respectively. The improvement for the OFF-state phase

TABLE III  
COMPARISON BETWEEN MEMRISTIVE SPDT TOPOLOGIES

Parameter	Topology		
	Series	Shunt <sup>1</sup>	Series-Shunt
Band of operation	Broad	Narrow	Broad
Control nodes	1	1	2
IL	$\sim 0.25$ dB	1 dB	$< 0.3$ dB
IS	$> 36$ dB	26 dB	$> 61$ dB
RL	$> 22$ dB	32 dB	$> 22$ dB
Area	Smaller	Larger	Medium

<sup>1</sup> Results at 30 GHz (designed frequency of the  $\lambda/4$ )

RMS error is 33%, and no improvement over the RC model is observed for the OFF-state magnitude. Furthermore, the switching dynamics measurements are fitted to the VTEAM model to predict the transient behavior. The obtained RMS error of this fitting is 1.53%.

The use of the proposed lumped model is demonstrated in three non-volatile single-voltage-controlled SPDT topologies. Design trade-offs are presented to further improve the RF performance of these devices. The topologies show high performance at high frequency. The proposed series-shunt topology increases the IS, maintains a low IL, with just a small area overhead. The non-volatility, small size, and low switching energy make these SPDTs strong candidates for use in communication systems and reconfigurable RF devices. Future work will focus on model validation with different data sets and RFMS devices, and on the fabrication and testing of the SPDT topologies for RF systems to perform a more accurate characterization and to compare them to MEMS-based and transistor-based SPDTs.

## ACKNOWLEDGMENT

The authors would like to thank Qiangfei Xia from UMASS, Amherst and his group for sharing experimental data and for his useful remarks. The authors would also like to thank N. Wald, L. Danial and T. Greenberg for their helpful comments.

## REFERENCES

- [1] A. Kaye and D. George, "Transmission of Multiplexed PAM Signals Over Multiple Channel and Diversity Systems," *IEEE Transactions on Communication Technology*, vol. 18, no. 5, pp. 520–526, October 1970.
- [2] B. D. Van Veen and K. M. Buckley, "Beamforming: A versatile approach to spatial filtering," *IEEE ASSP Magazine*, vol. 5, no. 2, pp. 4–24, April 1988.
- [3] G. M. Rebeiz, *RF MEMS: Theory, Design, and Technology*. John Wiley & Sons, 2003.
- [4] C. M. Ta, E. Skafidas, and R. J. Evans, "A 60-GHz CMOS Transmit/Receive Switch," *Digest of Papers of the IEEE Radio Frequency Integrated Circuits Symposium*, pp. 725–728, July 2007.
- [5] K. M. Naegle, S. Gupta, and D. J. Allstot, "Design Considerations for a 10GHz CMOS Transmit-Receive Switch," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2104–2107, July 2005.
- [6] S. Pi, M. Ghadiri-Sadrabadi, J. C. Bardin, and Q. Xia, "Nanoscale Memristive Radiofrequency Switches," *Nature Communications*, vol. 6, no. 7519, pp. 1–9, June 2015.
- [7] J. A. Nessel *et al.*, "A Novel Nanoionics-based Switch for Microwave Applications," *Proceedings of the International Microwave Symposium Digest*, pp. 1050–1054, June 2008.

- [8] A. Vena *et al.*, "A Fully Passive RF Switch based on Nanometric Conductive Bridge," *Proceedings of the International Microwave Symposium Digest*, pp. 1–3, June 2012.
- [9] L. O. Chua, "Memristor-The Missing Circuit Element," *IEEE Transactions on Circuit Theory*, vol. CT-18, no. 5, pp. 507–519, September 1971.
- [10] L. O. Chua and S. M. Kang, "Memristive Devices and Systems," *Proceedings of the IEEE*, vol. 64, no. 2, pp. 209–223, February 1976.
- [11] J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive Devices for Computing," *Nature Nanotechnology*, vol. 8, pp. 13–24, January 2013.
- [12] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM: Threshold Adaptive Memristor Model," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 1, pp. 211–221, January 2013.
- [13] S. Kvatinsky, M. Ramadan, E. G. Friedman, and A. Kolodny, "VTEAM - A General Model for Voltage Controlled Memristors," *IEEE Transactions on Circuits and Systems II, Express Briefs*, vol. 62, no. 8, pp. 786–790, August 2015.
- [14] J. J. Yang *et al.*, "Memristive Switching Mechanism for Metal/Oxide/Metal Nanodevices," *Nature Nanotechnology*, vol. 3, no. 7, pp. 429–433, July 2008.
- [15] Z. Bielek, D. Bielek, and V. Biolkova, "SPICE Model of Memristor with Nonlinear Dopant Drift," *Radioengineering*, vol. 18, no. 2, June 2009.
- [16] N. Wainstein and S. Kvatinsky, "An RF Memristor Model and Memristive Single-Pole Double-Throw Switches," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017, (in press).
- [17] Advanced Design System (ADS), Keysight Technologies, Santa Rosa, CA, USA, 2017. [Online]. Available: <http://www.keysight.com>
- [18] I. Valov, R. Waser, J. R. Jameson, and M. N. Kozicki, "Electrochemical metallization memories—fundamentals, applications, prospects," *Nanotechnology*, vol. 22, no. 25, p. 254003, May 2011.
- [19] R. Waser and M. Aono, "Nanoionics-based Resistive Switching Memories," *Nature Materials*, vol. 6, no. 11, pp. 833–840, November 2007.
- [20] N. El-Hinnawy *et al.*, "A Four-Terminal, Inline, Chalcogenide Phase-Change RF Switch Using an Independent Resistive Heater for Thermal Actuation," *IEEE Electron Device Letters*, vol. 34, pp. 1313–1315, October 2013.
- [21] N. El-Hinnawy *et al.*, "12.5 THz Fco GeTe Inline Phase-Change Switch Technology for Reconfigurable RF and Switching Applications," *2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, pp. 14–16, October 2014.
- [22] Y. Eo and W. R. Eisenstadt, "High-Speed VLSI Interconnect Modeling Based on S-Parameter Measurements," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 16, no. 5, pp. 555–562, August 1993.
- [23] A. Mazady and M. Anwar, "Memristor: Part II-DC, transient, and RF analysis," *IEEE Transactions on Electron Devices*, vol. 61, no. 4, pp. 1062–1070, April 2014.
- [24] M. D. Gregory and D. H. Werner, "Application of the Memristor in Reconfigurable Electromagnetic Devices," *IEEE Antennas and Propagation Magazine*, vol. 57, no. 1, pp. 239–248, March 2015.
- [25] E. Lehtonen and M. Laiho, "CNN using Memristors for Neighborhood Connections," *12th International Workshop on Cellular Nanoscale Networks and Their Applications (CNNA)*, pp. 1–4, February 2010.
- [26] W. Shu, S. Shichijo, R. Henderson, and X. An, "A Novel Model for Spiral Inductor based on a Unified CPW Circuit Model," *Proceedings of the Annual Wireless and Microwave Technology Conference*, pp. 1–3, July 2014.
- [27] W. Shu, H. Shichijo, and R. Henderson, "A Unified Equivalent-Circuit Model for Coplanar Waveguides With Silicon-Substrate Skin-Effect Modeling," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 6, pp. 1727–1735, May 2016.
- [28] R. N. Simons, *Coplanar Waveguide Circuits, Components, and Systems*. John Wiley & Sons, 2001.
- [29] S. P. Brooks and B. J. T. Morgan, "Optimization using simulated annealing," *Journal of the Royal Statistical Society Series D*, vol. 44, no. 2, pp. 241–257, 1995.
- [30] M. Kozicki, M. Yun, L. Hilt, and A. Singh, "Application of Programmable Resistance Changes in Metal-doped Chalcogenides," *Proceedings of the 1999 Symposium on Solid State Ionic Devices*, vol. 99, no. 13, pp. 298–309, February 1999.
- [31] J. N. Snyman, *Practical Mathematical Optimization: An Introduction to Basic Optimization Theory and Classical and New Gradient-Based Algorithms*. Springer Science & Business Media, 2005, vol. 97.
- [32] C. W. Chiu, "Capacitance Computation for CPW Discontinuities with Finite Metallization Thickness by Hybrid Finite-Element Method," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 4, pp. 498–504, April 1997.
- [33] I. Kallfass, S. Diebold, H. Massler, S. Koch, M. Seelmann-Eggebert, and A. Leuther, "Multiple-Throw Millimeter-Wave FET Switches for Frequencies from 60 up to 120 GHz," *European Microwave Integrated Circuit Conference (EuMIC)*, pp. 1453–1456, October 2008.
- [34] A. S. Cardoso *et al.*, "Low-loss, Wideband SPDT Switches and Switched-Line Phase Shifter in 180-nm RF CMOS on SOI Technology," *IEEE Radio and Wireless Symposium, RWS*, pp. 199–201, June 2014.
- [35] I. Valov and G. Staikov, "Nucleation and growth phenomena in nano-sized electrochemical systems for resistive switching memories," *Journal of Solid State Electrochemistry*, vol. 17, no. 2, pp. 365–371, Feb 2013.
- [36] S. Yu and H.-S. P. Wong, "Compact Modeling of Conducting-Bridge," *IEEE Transactions on Electron Devices*, vol. 58, no. 5, pp. 1352–1360, May 2011.
- [37] D. B. Strukov, "Endurance-write-speed tradeoffs in nonvolatile memories," *Applied Physics A: Materials Science and Processing*, vol. 122, no. 4, pp. 1–4, March 2016.
- [38] A. U. Zaman, M. Alexanderson, T. Vukusic, and P. S. Kildal, "Gap Waveguide PMC Packaging for Improved Isolation of Circuit Components in High-Frequency Microwave Modules," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 4, no. 1, pp. 16–25, January 2014.



**Nicolás Wainstein** received the Electrical Engineering degree from the Universidad de la República, Uruguay in 2014. From 2014 to 2015, he was a Research and Teaching Assistant with the Institute of Physics and the Institute of Electrical Engineering, Universidad de la República.

He is currently pursuing the Ph.D. degree at the Andrew and Erna Viterbi Faculty of Electrical Engineering, Technion - Israel Institute of Technology. His current research is focused on RF and analog circuits and systems using memristive devices.



**Shahar Kvatinsky** is an assistant professor at the Andrew and Erna Viterbi Faculty of Electrical Engineering, Technion - Israel Institute of Technology. He received the B.Sc. degree in computer engineering and applied physics and an MBA degree in 2009 and 2010, respectively, both from the Hebrew University of Jerusalem, and the Ph.D. degree in electrical engineering from the Technion - Israel Institute of Technology in 2014. From 2006 to 2009 he was with Intel as a circuit designer and was a post-doctoral research fellow at Stanford University from 2014

to 2015. Kvatinsky is an editor in Microelectronics Journal and has been the recipient of the 2015 IEEE Guillemin-Cauer Best Paper Award, 2015 Best Paper of Computer Architecture Letters, Viterbi Fellowship, Jacobs Fellowship, ERC starting grant, the 2017 Pazy Memorial Award, the 2014 and 2017 Hershel Rich Technion Innovation Awards, 2013 Sanford Kaplan Prize for Creative Management in High Tech, 2010 Benin prize, and six Technion excellence teaching awards. His current research is focused on circuits and architectures with emerging memory technologies and design of energy efficient architectures.