TIME—Tunable Inductors Using MEmristors

Nicolás Wainstein and Shahar Kvatinsky, *Member, IEEE*

***Abstract*— Memristors have proven to be an attractive feature for memory, logic-in-memory, and neuromorphic computing. Recently, radio-frequency memristive switches (RFMSs) have exhibited promising high-frequency performance, opening the possibility of their use in radio-frequency integrated circuit applications. In this paper, we present two novel topologies of Tunable Inductors using MEmristors, the memristive–via the switched tunable inductor and the multi-layer stacked inductor switched by an RFMS single-pole double-throw. The two inductor topologies are fully passive and are tuned by electrochemical metallization memristors. Memristive devices improve the performance of tunable inductors, as they provide low-area overhead, low-energy switching, and non-volatility, resulting in more compact and energy-efficient devices. The topologies are implemented and simulated in a momentum 3-D planar electromagnetic simulator. Simulation results show a maximum tunability of 296%, a quality factor of 18 at 5 GHz, and self-resonant frequency above 8.4 GHz.**

***Index Terms*— Memristors, tunable inductors, memristive devices, radio frequency, RFIC, tunable circuits, inductors, switches, monolithic wireless transceivers, wireless communications, Q-factor, self-resonant frequency.**

I. Introduction

INDUCTORS are fundamental passive devices in radio frequency integrated circuits (RFIC), extensively used in filters, tuned amplifiers and mixers [1]. Tunable inductors are valuable assets in frequency-division multiplexing (FDM) radios, tunable RF amplifiers and filters, voltage-controlled oscillators (VCO), software defined radios (SDR) and reconfigurable matching networks. These inductors become even more crucial when optimum tuning and impedance matching in a broadband range are desired, or when mismatches that arise from process variations must be fixed. Furthermore, tunable inductors can increase the flexibility, adaptability and reliability of radio transceivers.

Discrete and continuous variable (or tuned) inductors using microelectromechanical systems (MEMS) and transistors are both reported in the literature [2]–[5]. The main drawbacks of MEMS tunable inductors are substantial area overhead, degradation due to moving mechanical parts, high actuation voltages, and a costly and complex fabrication process. Contrariwise, the main disadvantages of reconfigurable inductors using transistors include large parasitic capacitance and high ON resistance, which result in, respectively, self-resonant frequency (SRF) reduction and decrease of the quality factor (Q). Furthermore, transistors add a non-negligible static power consumption to the passive inductor.

Memristors and memristive devices are two terminal passive circuit elements, whose resistance is determined by the history of the applied voltage or current and retained whenever the voltage or current is no longer applied (*i.e.*, non-volatility) [6], [7]. These devices exhibit nonlinear behavior. Therefore, they can be used as switches with a low resistive state (LRS, R_{ON}) and a high resistive state (HRS, R_{OFF}). Switching from HRS to LRS is denoted as SET, while the opposite switching direction is called RESET. The switching mechanism depends on the technology of each memristor, though it is typically determined by the formation or rupture of conductive filaments between two electrodes in a metal–insulator–metal (MIM) structure [8]. In other words, the switching mechanism is actually a change in the device structure.

Their non-volatile, small footprint, scalability, high endurance and fast switching capabilities make memristors an attractive feature for memory, logic within memory [9] and neuromorphic computing [10]. Recently, RF memristive switches (RFMS) have been proposed [11]–[13], opening the possibility for a wide range of applications in RFIC.

In this paper, we present two different topologies of tunable inductors using memristors (TIME). Because tuning is done by an actual change in the structure of the inductor, there are no moving mechanical parts. The added non-volatility and the low-energy switching reduce the power consumption; the small footprint allows further scaling, hence improving the density in, for example, massive multiple-input multiple-output (MIMO) radio transceivers. The topologies are designed and simulated in Advanced Design System (ADS) from Keysight Technologies [14], and evaluated for their achievable inductance, tunability (*i.e.*, potential variation from the nominal value), Q, SRF, area overhead, and complexity.

This paper is organized as follows. In Section II, RFMS and tunable inductors are reviewed. In Section III, the memristive–via switched tunable inductor is presented. The second topology, the multilayer stacked inductor (MSI) tuned by RFMS single-pole double-throw (SPDT) is introduced in Section IV. In Section V, a comparison between the two TIME topologies and between TIME and other tunable inductors is presented. The paper is summarized in Section VI.

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The authors are with the Andrew and Erna Viterbi Faculty of Electrical Engineering, Technion–Israel Institute of Technology, Haifa 32000, Israel (e-mail: nicolasw@campus.technion.ac.il; shahar@ee.technion.ac.il).

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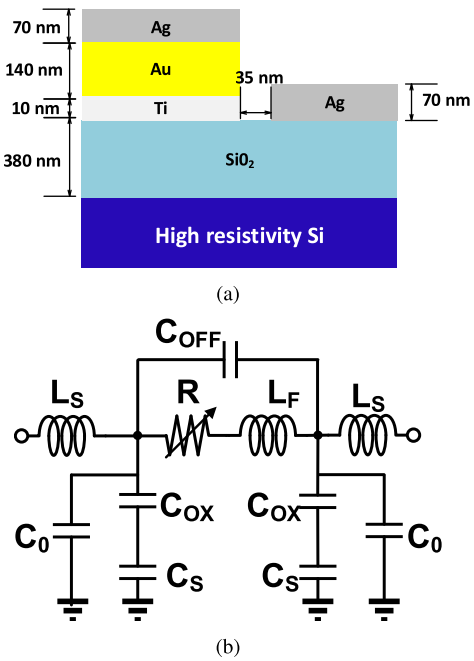


Fig. 1. (a) Physical structure schematic of the RFMS proposed in [11]. Two metal electrodes (Ag and sandwiched Ti/Au/Ag respectively) separated by a 35 nm air gap are placed in-line on a CPW. (b) Lumped RF memristive switch model [17], where R and C_{OFF}, represent the memristance and the gap capacitance ($i.e.$, the capacitive coupling effect between the electrodes), respectively. Inductor L_F is the inductance of the filament, inductors L_S are the inductances of the electrodes, capacitor C_{ox} represent the SiO_2 parasitic capacitance, C_s is the Si substrate capacitance, and C_0 is the fringe capacitance between the signal line and ground planes.

II. Background

A. RF Memristive Switches

RF switches require both low resistance in the ON state and low capacitance in the OFF state to achieve low insertion loss (IL) and high isolation (IS) [15], respectively. Consequently, most of the proposed RFMS in the literature are ECM memristors, consisting of a pair of electrochemically asymmetric metal electrodes separated by a small-scale gap or an ion-conducting insulating layer [8]. This technology exhibits one of the lowest LRS in the memristive device playground and R_{ON} is linearly dependent on the compliance current [16]. In a first order approximation, the memristor can be modeled as a parallel RC circuit, where R accounts for the memristance ($i.e.$, resistive states) and C stands for the between-electrodes, or OFF capacitance (C_{OFF}). Higher order effects include, for instance, losses and capacitive coupling to the substrate [17].

In [11], an ECM with Ag and Ti/Au/Ag electrodes (active and inert, respectively) separated by a 35 nm air gap is presented. The device is fabricated over a SiO_2 surface in a high resistivity silicon substrate, in Coplanar Waveguide (CPW) transmission line. A schematic of the device structure is shown in Fig. 1(a). Unlike typical crossbar structures, this device is horizontally settled. The reported device presents an R_{ON} of 2.6 Ω, an R_{OFF} in the order of 1 $T\Omega$, and a C_{OFF} of 1.41 fF. The LRS and HRS are achieved by applying, respectively, 3 V and -0.4 V across the terminals.

Another RFMS, introduced in [13], consists of a 10 μm gapless-type ECM with Ag and Ni electrodes (active and inert, respectively). Measurements from 1 to 6 GHz demonstrate an IL of less than 0.5 dB and an IS better than 30 dB (R_{ON}, R_{OFF} and C_{OFF} are not reported). The necessary voltage/current to change the state of the device is nominally 1 $V/10$ mA (SET) and -1 $V/10$ mA (RESET). In [12], a $Cu/SiO_2/Al$ gapless-type ECM RFMS is proposed. This switch is characterized at 0.15 GHz, achieving an IL of 1.6 dB and an IS of 20 dB (R_{ON}, R_{OFF} and C_{OFF} are not reported). Although its performance is lower than that of the aforementioned RFMS, it nonetheless stands out for its simple structure, and therefore its simpler fabrication process.

Another family of RFMS are phase change materials (PCM)-based switches. The switching mechanism in these devices relies on transitioning between the amorphous (insulating) and crystalline (conductive) states of a chalcogenide, which is accomplished by heating and cooling the PCM. In [18] and [19], inline PCM RF switches are presented. These switches can achieve an R_{ON} of 4.5 Ω and a C_{OFF} of 35 fF. These devices require a significantly larger area than ECM switches, provide a lower isolation, the programming voltages exceed 10 V, and for some compounds the device is required to be kept above a certain temperature to retain the LRS ($e.g.$, 67°C for VO_2).

B. RFMS Modeling

In previous work [17], we proposed a novel model based on examination of the structure of the memristive device presented in [11], as shown in Fig. 1(b). This model relies on the voltage threshold adaptive memristor (VTEAM) model [20] for transient analysis ($i.e.$, describes the programming sweep) and introduces a structure-inspired lumped RLC circuit to describe its behavior at high frequency. VTEAM is a flexible and general model that accurately describes voltage controlled memristive devices and relies on a voltage threshold parameter. The derivative of the internal state variable x is

$$\frac{dx}{dt} = \begin{cases} k_{on}\left(\dfrac{v(t)}{v_{on}} - 1\right)^{\alpha_{on}} f_{on}(x), & v < v_{on} < 0, \\ 0, & v_{on} < v < v_{off}, \\ k_{off}\left(\dfrac{v(t)}{v_{off}} - 1\right)^{\alpha_{off}} f_{off}(x), & 0 < v_{off} < v, \end{cases} \tag{1}$$

where k_{on}, k_{off}, α_{on}, and α_{off} are fitting parameters. Voltages v_{on} and v_{off} are the ON and OFF threshold voltages, respectively. Functions $f_{on}(x)$ and $f_{off}(x)$ describe the relation between the derivative of the state variable and the state variable x. These functions are window functions which bound the internal state variable between $[x_{on}, x_{off}]$. The current-voltage relationship is

$$i(t) = \left[R_{ON} + \frac{R_{OFF} - R_{ON}}{x_{off} - x_{on}}(x - x_{on})\right]^{-1} v(t). \tag{2}$$

In Fig. 1(b) the parameters R, L_F and C_{OFF} represent the memristance, the inductance of the filament, and the gap capacitance, respectively. Capacitor C_{ox} represents the SiO_2

TABLE I
MODEL PARAMETERS

Parameter	Fitted value
R_{ON}	2.6 Ω
C_{OFF}	1.145 fF
C_p	3.08 fF
L_F	77 fH
L_S	3.7 pH

parasitic capacitance, C_s is the Si substrate capacitance, and C_0 is the fringe capacitance between the signal line and the ground planes. These capacitors can be described by a single equivalent capacitor, C_P. Note that if the memristor is implemented in a microstrip structure, there will be no fringe capacitance C_0. Finally, inductors L_s are the inductance of the electrodes.

This model is used in Section IV as part of an RFMS SPDT to switch between different spirals of a multi-layer stacked inductor (MSI). The fitted model parameters from measurement data obtained from [11] are listed in Table I.

C. Tunable Inductors and Their Applications

Monolithic tunable inductors are widely used in RFIC applications (*e.g.*, amplifiers, VCO and filters). Integrated inductors are generally implemented as metal spirals to take advantage of the mutual inductance between two (and more) turns. The key parameters of their design are the number of turns N, outer diameter, width of the conductor, and spacing between loops. Inherent problems of monolithic inductors are their low Q and low SRF. If an inductor is modeled by a simple parallel RLC tank, Q and SRF are defined [21], respectively, as

$$Q = \frac{R_P}{\omega L_P}, \tag{3}$$

$$SRF = \frac{1}{\sqrt{L_P C_P}}, \tag{4}$$

where R_P, L_P and C_P are, respectively, the equivalent parallel resistance, inductance, and capacitance of the inductor. To reduce the resistance of the metal wires, the spiral is implemented in the top metal layer since it is the thickest layer.

To gain a better understanding of the extent of tunable inductors, consider a simplified topology of a common-source (CS) inductively-degenerated cascode low noise amplifier (LNA) as illustrated in Fig. 2. Since the CS topology is conditionally stable in nature (*i.e.*, it is not stable for all frequencies) due to C_{gd}, the gate-drain capacitance, inductor L_S is added to obtain *inductive source degeneration* [22], thus granting stabilization and matching. Neglecting the body-effect and channel-length modulation, the input impedance seen from the power source is given by

$$Z_{in} \simeq \frac{1}{j\omega C_{gs_1}} + j\omega(L_S + L_{in}) + \frac{g_m L_S}{C_{gs_1}}, \tag{5}$$

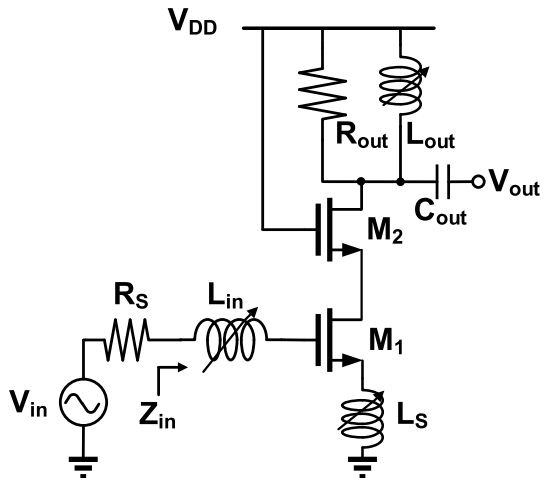


Fig. 2. Simplified common-source inductively-degenerated cascode LNA. Resistance R_s is the source resistance. Inductors L_{in} and L_s provide input impedance matching and stabilization. The output matching network consists of R_{out}, L_{out} and C_{out}.

where C_{gs_1} and g_m are, respectively, the gate-source parasitic capacitance and the small-signal transconductance of transistor M_1. Note that the third term in (5) is a positive frequency-independent impedance. Hence, it can be designed to be 50 Ω to match the source output resistance. Inductor L_{in} can be designed to resonate (together with L_s) the capacitance C_{gs_1} at the desired operating frequency, eliminating the undesired reactance. Moreover, capacitor C_{out} and inductor L_{out} form an L-matching network to match the output.

In a scenario where the aforementioned inductors could vary, a variable gain amplifier (VGA) is straightforwardly obtained. Thus, this amplifier can be stabilized and matched at multiple frequencies and/or different bias voltages. In low-power, energy harvesting systems or multi-band devices where, the correspondingly, input voltage or operating frequency vary, performance of classic tuned amplifiers drops drastically owing to input and output mismatches, which could even lead to instability. Contrariwise, an amplifier with tunable inductors can be configured to obtain optimal matching, consequently enhancing its efficiency.

Possible drawbacks are area overhead, increased power consumption, extra complexity, and Q and SRF degradation related to the added switching devices. The promising characteristics of RFMS can ease this trade-off: small footprint, small parasitic capacitance, low-energy switching, non-volatility, and highly integration capabilities.

III. MEMRISTIVE–VIA SWITCHED TUNABLE INDUCTOR

In this section the memristive–via switched tunable inductor is introduced. First, we present the device operation, followed by design and methodology considerations for its implementation and evaluation. Then, we discuss possibilities to further enhance the tunability of this TIME topology. Finally, simulation results are presented.

A. Operation

In a memristive crossbar array, memristors are built within the inter-wire junction of two adjacent-layer, perpendicularly

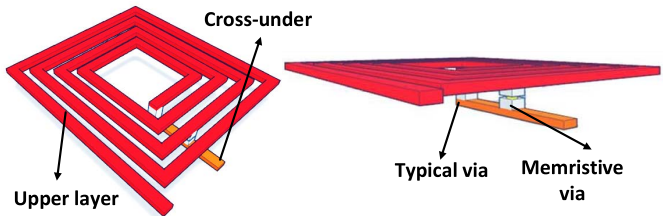


Fig. 3. 3D schematic illustration of the memristive–via switched tunable inductor. The spiral is implemented in the upper layer (in red), a typical via connects it with the cross-under conductor (in orange) and a memristor provides a second possible connection between the two layers.

routed nanowires [23]. Here, we propose to use the same concept to connect and disconnect, in different locations, the top layer and cross-under layer of a monolithic spiral inductor. Thus, memristors act as switchable vias and there is no need for routing to lower metal layers (MLs). By switching their state, both the effective total length and N are changed. As a result, the self-inductance and the mutual inductance change, tuning the total inductance. A 3D representation of a square spiral inductor using one memristive via is shown in Fig. 3. The spiral is implemented in the upper metal layer, which provides the lowest resistance of the back-end of line (BEOL) metal layers owing to its thickness. The cross-under conductor is connected to the upper layer through one via at the center of the spiral and through a memristor at another intersection.

Thus, for the exhibited inductor, the effective number of turns can be tuned from four to two by changing the state of the memristors from HRS to LRS, respectively. The added memristor does not increase the area of the inductor. However, an additional control mechanism must be included to manage the memristor, adding an area overhead only in the transistor layer.

A simple model of this TIME topology is shown in Fig. 4(a), where L_i is the inductance of each loop in the spiral and R_{VIA} is the resistance of the central via. The parasitic capacitances (*e.g.*, to the substrate and between the spiral and the cross-under) and the resistance of the conductor are C_i, C_{S_i} and R_i, respectively. A cross-section schematic illustration of the device is shown in Fig. 4(b). The functionality of this topology relies on the following condition,

$$R_{ON} \ll R_2 + R_{VIA} \ll R_{OFF}, \tag{6}$$

where R_2 is the resistance of the remaining spirals, *i.e.*, the inner loops. Memristor M_1 is connected between the top layer and the cross-under and acts as a switchable via. When M_1 is in HRS, the current flowing through it can be neglected; hence, at low frequency the input impedance is determined by

$$Z_{in} = j\omega(L_1 + L_2 + 2\overline{M}_{L1,L2}) + R_1 + R_2 + R_{VIA}, \tag{7}$$

where $\overline{M}_{L1,L2}$ is the mutual inductance between the different loops. Alternatively, when memristor M_1 is in LRS it provides a low impedance path, and the current flowing to the second circuit loop is negligible. Hence, the input impedance in this cases is expressed by

$$Z_{in} = j\omega L_1 + R_1 + R_{ON}. \tag{8}$$

B. Design, Methodology and Simulations

The following characteristics of memristors make them well-suited to operate as switchable vias: (a) a low R_{ON}, which provides a low impedance path to the cross-under (*i.e.*, smaller than the resistance of the remaining wire loops together with the remaining via), making it possible to effectively change the inductance and obtain an acceptable Q; (b) a relatively high R_{OFF} (in the order of $k\Omega$) to isolate the terminals; and (c) a small C_{OFF} (in the order of pF) for reduced capacitive coupling between the terminals. Namely, memristors as switchable vias share the same characteristics as an RFMS.

The reduced C_{OFF} constraint can be difficult to achieve considering that most insulators in vertically-oriented MIM structures have high dielectric constants. To reduce the capacitance, either the distance between the electrodes must be increased or the cross-section of the electrodes reduced. Alternatively, vacuum or polymer filled gap-type ECM memristors [16] can be used. However, the aforementioned changes may vary the SET/RESET threshold voltages (namely, V_{SET} and V_{RESET}) and the LRS/HRS resistance values. Thus, these modifications must be meticulously studied. Finally, we assume that no self-switching occurs at the band of interest and that switching occurs when no RF signal is applied (*i.e.*, cold-switching).

The memristive–via switched tunable inductor is implemented and simulated in a 1P6M RF CMOS substrate in ADS, modified to simulate the memristor structure. The material composition of vias from ML5 to ML6 and from ML4 to ML5 is changed to be the same as in an ECM structure (namely, Ag and Au for the upper and bottom electrodes, respectively). Furthermore, the height of layer 5 is reduced to 15 nm and the material composition of the via from ML4 to ML3 is defined to have three times the resistance of bulk Ag to simulate the filament and account for nanoscale effects as in [11]. The aforementioned via is implemented with a section diameter of 100 nm as in [11]. Moreover, for the sake of providing a better sustain, the air-gap in [11] is filled with a chalcogenide passivation layer as in [13] (*i.e.*, Ag^+-saturated $GeSe_2$). Thus, the insulator material for this layer is chosen to be a chalcogenide with an approximate dielectric constant, ε, equal to eleven.

The square spiral is implemented in ML6 with an outer diameter of 160 μm, conductor width of 5 μm, between loops spacing of 2 μm and six turns. The cross-under conductor is implemented in ML3 with same width. States LRS and HRS of the memristor are simulated, respectively, as the presence or absence of the filament. This methodology is supported by the concept of 'winner takes it all' [24], meaning that a single conductive filament will determine the resistance in LRS.

For simulation purposes, inductance and Q are defined as in [25],

$$L = \frac{Im\{1/Y_{11}\}}{\omega}, \tag{9}$$

$$Q = \frac{Im\{1/Y_{11}\}}{Re\{1/Y_{11}\}}, \tag{10}$$

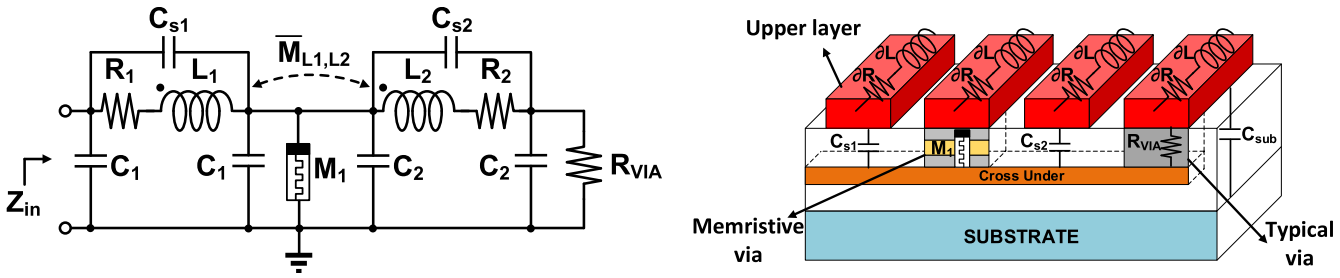


Fig. 4. (a) Equivalent circuit model of the memristive–via tuned inductor. The two RLC circuits represent the two sections of the spiral inductor. Capacitors C_1 and C_2 represent the capacitive coupling of the loops to the substrate, and resistors R_1 and R_2 are the resistance of the loops. Capacitors C_{S_1} and C_{S_2} represent the coupling capacitance between the upper layer and the cross-under. R_{VIA} is the resistance of the central via and M_1 is the memristor-via (the memristor model is not shown). Inductors L_1 and L_2 are the self-inductance of the loops and $\overline{M}_{L1,L2}$ is the mutual inductance between the two inductors. (b) Cross-section of the memristive–via tuned inductor showing the lumped elements that form the equivalent model. Parameters ∂R and ∂L are the sheet resistance and sheet self-inductance of the loops, respectively. Capacitor C_{sub} represents here the capacitive coupling to the substrate (which form C_1 and C_2 in (a)).

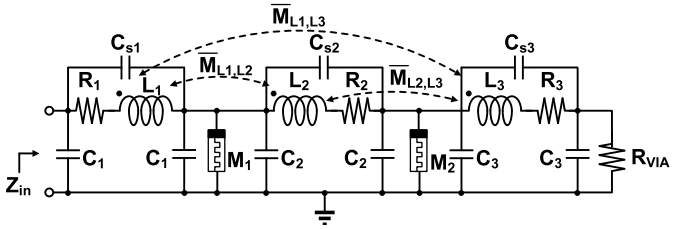


Fig. 5. Equivalent circuit model of the memristor–via tuned inductor using two memristors (M_1 and M_2) for multiple steps. Capacitors C_i represent the capacitive coupling to the substrate of the different turns, resistances R_i are the resistance of the loops. Capacitors C_{S_i} represent the coupling capacitance between the upper-layer and the cross-under for different turns. R_{VIA} are the resistance of the central via and R_i is the resistance of the different loops. Inductor L_i is the self-inductance of the loops and $\overline{M}_{Li,Lj}$ is the mutual inductance between inductors L_i and L_j.

where Y_{11} corresponds to the input impedance in a Y-parameter circuit model. The SRF is determined by the frequency at which the spectral response of L crosses zero. At this specific frequency the inductive reactance equals the capacitive reactance of the inductor (*i.e.*, resonance).

C. Programming and Adding Further States

The memristor stands between two conductors; hence the low-frequency programming signals can be supplied through the inductor itself, using the same ports as those for RF signals. However, this restricts the number of states that can be achieved, since similar voltages will drop on every memristor if the resistance between them is small. In Fig. 5, an equivalent model with two memristive–vias is shown. Note that due to resistances R_1, R_2, R_3 and R_{VIA} and the state of both memristors M_1 and M_2, the voltage drop across M_2 will be smaller than the voltage drop across M_1. The voltage drop at low frequency in M_1 is

$$V_{M_1} = V_{in}\frac{R_{eq_1}}{R_{eq_1} + R_1}, \tag{11}$$

where $R_{eq_1} = M_1||\left(R_2 + R_{eq_2}\right)$ and $R_{eq_2} = M_2||(R_3 + R_{VIA})$. Conversely, the voltage drop at M_2 is

$$V_{M_2} = V_{M_1}\frac{R_{eq_2}}{R_{eq_2} + R_2}. \tag{12}$$

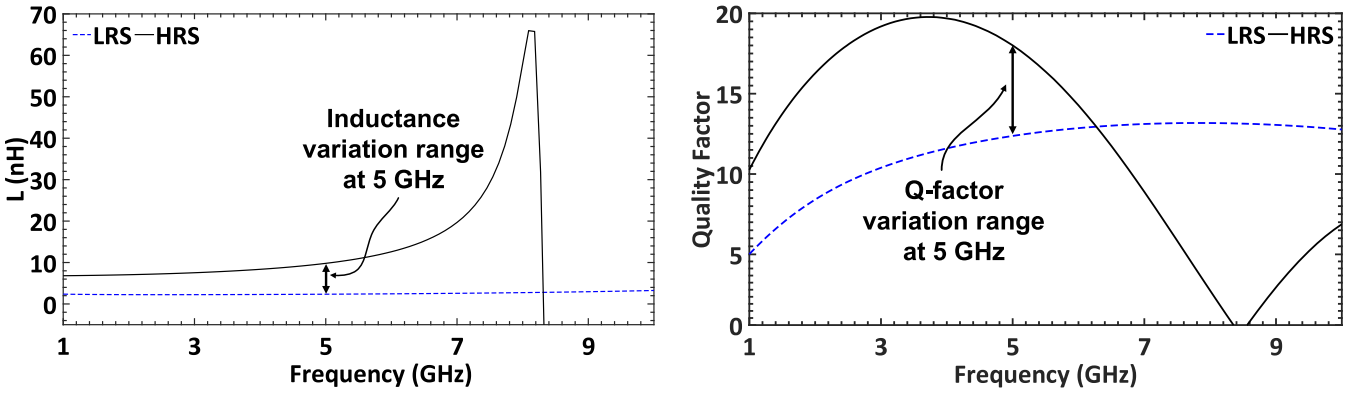
In this configuration, a particular protocol is required to correctly program the device. To SET only M_1, $V_{M_1} \geq V_{SET}$, and similarly for RESET, $|V_{M_1}| \geq |V_{RESET}|$. However, if initially M_2 is in LRS, a previous step should be to RESET M_2, followed by a SET step as mentioned before. Conversely, to only SET M_2, the first step is to SET both memristors and then RESET M_1. Note that when applying an input voltage such that $V_{M_1} = V_{RESET}$, the voltage drop in M_2 is $V_{M_2} < |V_{RESET}|$, and it is not reset.

The drawback of this implementation is the reduction of SRF owing to the increased parasitic capacitance in the inductor. Moreover, the number of achievable steps is limited by discriminability of the voltage drop in each memristor. This margin is related to the value of resistance R_i (loop resistance between two memristors), the maximum input current that can be sustained by the MLs, and the resolution of the controller (*i.e.*, the minimum discrete voltage step that it can provide). If these resistances decrease, either due to improvements on the BEOL metal layers (*i.e.*, lower resistance) or owing to closely placed memristors, almost equal voltage will drop on each. In this scenario, there is no way to program an individual memristor.

A completely different approach is to exploit the dependence of LRS on the compliance current [26] during the SET operation. When the compliance current is further increased, a lower LRS is achieved due to filament diameter widening. Thus, if this current can be controlled with fine-grained resolution or quasi-continuum values, multiple states or continuous values of inductance can be programmed. Possible drawbacks of this methodology are the variability of R_{ON} due to process variations and possible damage due to Joule heating caused by high currents. Therefore, an additional mechanism to control this value is required. Different approaches for multi-level programming are presented in [27]–[29].

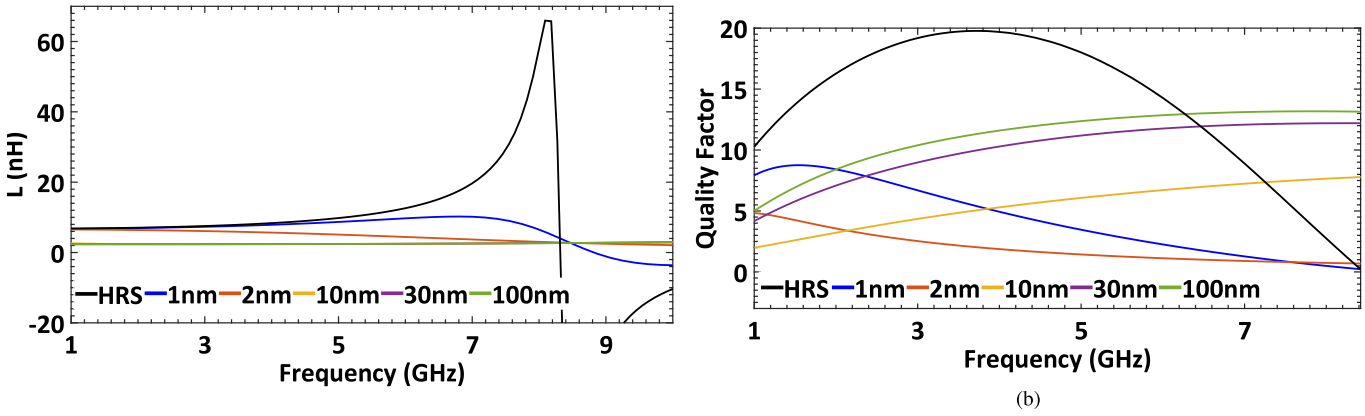
D. Results

This TIME topology is evaluated by its inductance, Q and SRF. The frequency response of the inductance and Q for the memristive–via switched tunable inductor are shown, respectively, in Fig. 6(a) and Fig. 6(b). The simulation results at 5 GHz are listed in Table II. It can be observed that when



(a) (b)

Fig. 6. Simulation results for the memristor–via tuned inductor using a single memristor. Frequency response according to the state of the memristor (LRS/HRS) for the (a) Inductance and (b) Q.



(a) (b)

Fig. 7. Simulation results for the memristor–via tuned inductor varying the width of the filament. Frequency response according to the width of the filament (HRS represents the absence of the filament). (a) Inductance, (b) Quality factor.

TABLE II
RESULTS AT 5 GHz FOR MEMRISTIVE–VIA SWITCHED TUNABLE INDUCTOR

Memristor's state	$L\ (nH)$	Q	$SRF\ (GHz)$
HRS	9.6	18	8.4
LRS	2.43	12.4	20.5

the memristor is at HRS, both the inductance and the Q are higher than for the LRS. The change in L is explained by the change in the total length and the change in N. The former affects the contribution of the self-inductance of the conductors and the latter causes the mutual inductance between turns to vary, as theoretically described by (7) and (8). Furthermore, Q decreases at LRS due to an inferior ratio between the inductive part and the resistive part of the impedance. This is related to the aforementioned decrease in L, as well as to a relative increment in the resistance owing to longer loops ($i.e.$, the outer loops are longer than the inner loops), and the added R_{ON} of the memristor.

The SRF is also altered by the change in the state of the memristor, still in the opposite direction, changing from 8.6 GHz at HRS to 20.5 GHz at LRS. When the memristor is in HRS, the total parasitic capacitance of the inductor is more significant owing to a larger area. Hence, the SRF decreases considerably as described by (4). Still, the SRF at HRS is sufficiently high to ensure its operation at WiFi frequencies ($i.e.$, 2.4 and 5 GHz). The SRF can be improved by reducing the width of the conductor, which results in smaller parasitic capacitance. However, this will further reduce Q; thus this design tradeoff depends on which of these two parameters is more critical to the specific application.

Results of the frequency response of the inductance and Q while varying the width of the filament are shown in Fig. 7(a) and 7(b), respectively. State HRS, as mentioned before, is implemented as the absence of the filament. The diameter of the filament is changed from 1 nm to 100 nm to exhibit the possibility of continuous change in the inductance by modulating the compliance current. Whereas a diameter of 10 nm already switches to the low L value, and equals the achieved inductance for 100 nm, it can be observed in Fig. 7(b) that Q is degraded when the diameter of the filament decreases.

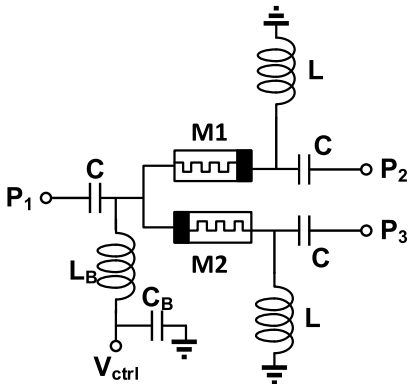


Fig. 8. Schematics of the series SPDT RFMS [17]. Capacitors C are DC blockers and RF feeds, while L_B and C_B are part of a bias-tee.

IV. Multi-Layer Stacked Inductor Tuned by SPDT RFMS

In this section, we present another tunable inductor topology: a multi-layer stacked inductor (MSI) tuned by a SPDT RFMS. First, we explain the operation of an SPDT RFMS, which provides tuning capabilities to an MSI. Then, we describe the operation of this TIME topology, followed by a description of the design, methodology and simulations. Finally, the results are presented, showing enhanced inductance tunability at the expense of lower Q with respect to the previously described topology.

A. SPDT RFMS

In previous work [17], we proposed two SPDT RFMS topologies, series and shunt. These switches exhibit high performance in RF, can be programmed using only a single bias signal, and provide non-volatility to SPDT RF switches, thus reducing the number of bias operations and the energy consumption compared to other technologies (*e.g.*, MEMS, transistors and PIN diodes). The series topology, shown in Fig. 8, exhibits improved performance compared to the other topologies, as it provides both lower IL and higher IS, while requiring less area.

Memristors M_{1-4} are modeled as described in Section II-A. Owing to the opposite-polarity connection, the SPDT operation is as follows. Memristor M_1 switches to LRS and M_2 to HRS when applying $V_{ctrl} = -3\ V$, hence providing a conductive path for the RF signal from port P_1 to port P_2, while P_3 is isolated. An analogue analysis is done when $V_{ctrl} = 3\ V$.

B. Operation of the MSI

MSIs have been reported in the literature since the '90s due to their enhanced inductance per area [21]. In this paper, we propose to use an adapted version of the series SPDT RFMS to switch between different inductors placed in a stacked manner as illustrated in Fig. 9. The two spiral inductors are connected in series through a central via. To enable tunability, another port is added and connected to this central via. Thus, when connecting the RFMS SPDT, the circuit can be modeled as in Fig. 10, where L_1 and L_2 are,

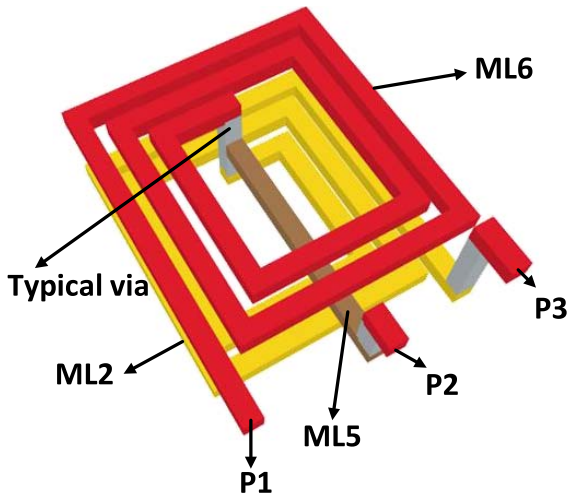


Fig. 9. 3D schematic illustration of the implemented MSI. Lower-layer spiral in ML2 (yellow), additional port in ML5 (green), and upper-layer spiral in ML6 (red). The device has three ports accessible from the upper layer (P_1, P_2, P_3), where the SPDT is connected to switch between two possible inductance levels. The layers are connected with vias (gray).

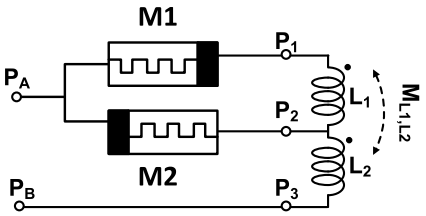


Fig. 10. Equivalent circuit model of a MSI tuned by an RFMS SPDT. Inductor L_1 is the upper-layer inductor, L_2 is the lower-layer inductor. $M_{L1,L2}$ is the mutual inductance between the two inductors. The parasitic capacitances and resistance, and the bias tee are not included in this schematic.

respectively, the upper-layer and lower-layer spiral inductors. Ports P_2 and P_3 of the series SPDT are connected to the MSI at P_1 and P_2, respectively, and accessed externally through P_A. Port P_3 is accessed externally through P_B. Using the series SPDT is preferable to the shunt topology because the latter requires a quarter-wavelength transformer, which adds a significant resistance and thus considerably reduces the Q of the inductor. Employing a single memristor in parallel to a single loop (*i.e.*, to bypass it at LRS) also reduces the Q as some of the current flows through the bypassed inductor and the effective inductance is reduced. For this application, the SPDT capacitors and inductors are not required (see Fig. 8). The ground reference is given by the MSI itself, and there is no need for DC block capacitors since only RF signals flow through the inductor after programming the memristors.

We define S1 as the state where M_1 is in LRS (M_2 in HRS) and S2 as the state where M_1 is in HRS (M_2 in LRS). For S1 the total inductance is expressed as

$$L = L_1 + L_2 + 2\overline{M}_{L1,L2}, \tag{13}$$

where $\overline{M}_{L1,L2}$ is the mutual inductance between the two spiral inductors. Assume L_1 and L_2 are almost identical (*i.e.*, the two loops are identical, except for the height of the conductor)

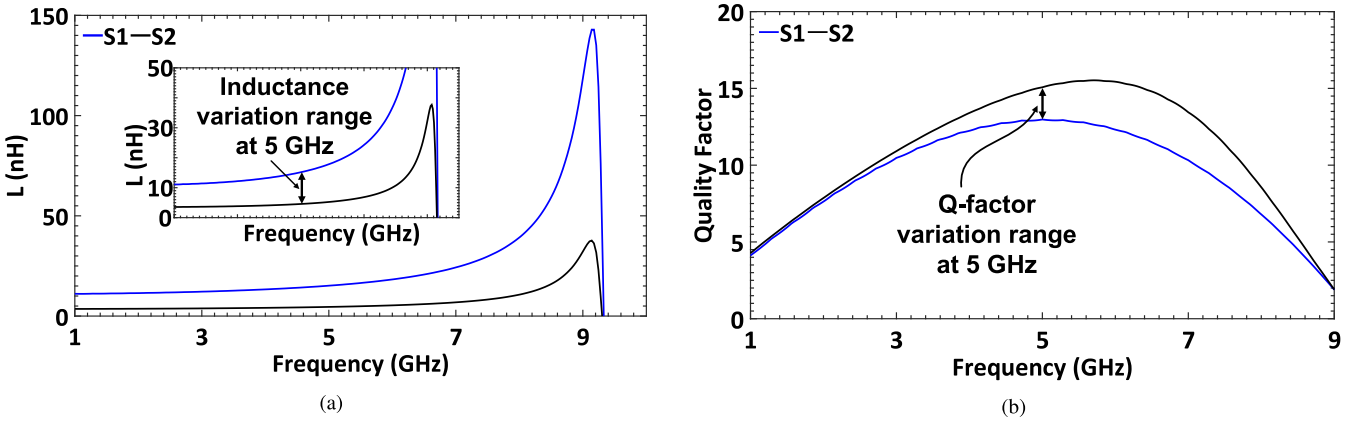


Fig. 11. Simulation results for the MSI tuned by SPDT RFMS. Frequency response for states S1 and S2. (a) Inductance (inset shows a detailed view around the frequency of interest), (b) Q.

and $\overline{M}_{L1,L2} = k\sqrt{L_1\ L_2}$, where k is the coupling coefficient, $0 \leq k \leq 1$. Then (13) can be expressed as

$$L_{S_1} \simeq (2 + 2k)L_1. \tag{14}$$

For S2 the total inductance is simply

$$L_{S_2} = L_2. \tag{15}$$

This topology introduces an area overhead since memristors are located horizontally in the upper layer as in [11] and extra routing wires are needed. Only a single bias signal is used to program the device, and a ground reference (or DC voltage reference) must be provided. Port P_B could be used for that purpose, and many applications require one terminal of the inductor to be connected in this manner. Whenever the circuit lacks a reference voltage, an extra device (*e.g.*, a transistor) should connect this terminal to ground in order to program the memristors.

To improve tunability (*i.e.*, additional inductance states), another spiral inductor in ML4 together with another RFMS SPDT can be added. These changes provide two additional states. However, a slight area overhead arises owing to the added bias signals required to control the additional SPDT.

C. Design, Methodology, and Simulations

The tunable MSI is implemented in a 1P6M substrate in ADS. The upper-layer spiral inductor is implemented in ML6, as it is the thickest and less resistive layer. The middle port, P_2, is routed in ML5 and the lower spiral inductor is implemented in ML2 to reduce the parasitic capacitance between the upper spiral and lower spiral inductors. This technique has proven to significantly increase the SRF in stacked inductors [21]. Both inductors have an outer diameter of 160 μm, conductor width of 5 μm, loop spacing of 2 μm, and six turns. The topology is simulated at a schematic level by extracting an electromagnetic model from the layout of the inductor, and by connecting it to the RFMS SPDT. For this TIME topology, the inductance and the Q are also calculated as (9) and (10), respectively. The states of M_1 and M_2 are switched to select the different spirals. The SRF is determined in the same manner as explained in Section III-B.

TABLE III
RESULTS AT 5 GHz FOR THE MSI TUNED BY SPDT RFMS

State	$L\ (nH)$	Q	$SRF\ (GHz)$
S1	15.3	12.7	9.3
S2	4.6	14.6	9.3

D. Results

As for the first presented TIME topology, the MSI tuned by RFMS SPDT is evaluated by its inductance, Q and SRF. The frequency response of the inductance and the Q are shown, respectively, in Fig. 11(a) and Fig. 11(b). The simulation results at 5 GHz are listed in Table III. It can be seen that in S1 the inductance is more than 3× the inductance in S2, increasing from 4.6 nH to 15.3 nH. From (14), it can be derived that $k = 0.66$ and thus $L_{S_1} \simeq 3.3L_1$.

In S1, Q is slightly lower than in S2 due to the substantial increment in the total length of the loops, which effectively decreases the ratio between the reactance and impedance. Nevertheless, both states provide sufficient Q for many RFIC applications. With regard to the SRF, both states exhibit approximately the same resonant frequency owing to equal parasitic capacitance.

V. DISCUSSION

In this section, we first compare between the two proposed TIME topologies by considering different metrics. Then, we compare TIME to previously reported tunable inductors implemented with other technologies.

A. Comparison Between the Two TIME Topologies

To conduct a fair comparison between the two TIME topologies, all spiral inductors are implemented with equal dimensions. Moreover, we define a Tunability Range (TR) as

$$TR = \frac{L_{max} - L_{min}}{L_{min}}. \tag{16}$$

The results of this comparison are listed in Table IV. The MSI provides higher inductance at the expense of lower

TABLE IV
COMPARISON BETWEEN THE TWO TIME TOPOLOGIES

Topology	Max. L (nH) at $5\ GHz$	Max. Q at $5\ GHz$	SRF (GHz)	TR	Area overhead	Complexity of adding further steps	Complexity of fabrication
Memristive–via switched tunable inductor	9.6	18	8.4 & 20.5	3.95	None	Limited by the series resistance value	At least three more steps to add electrodes and insulator [1]
MSI tuned by SPDT–RFMS	15.3	14.6	9.3	3.3	RFMS SPDT and routing	Limited by the number of layers	The RFMS could be added in post-processing

[1] Two if one of the electrodes is made of the same material as the spirals

TABLE V
COMPARISON BETWEEN TIME AND OTHER TUNABLE INDUCTORS

Tunable inductor	Type	Advantages	Disadvantages	TR%	Area overhead[1]	No. of states	No. of bias
Memristive–via switched tunable inductor	Memristive–via	No area overhead, middle-high Q, achievable multiple or quasi-continuum L values	Need for a complex controller to achieve multiple L values	295.5	None	≥ 2	1
MSI tuned by SPDT RFMS	SPDT RFMS	Use of existent memristive device, middle-high Q and L	Area overhead	232.6	RFMS SPDT and their routing to the MSI	2	1
[3]	Mutual inductance switched by MEMS relays	High Q, post-process CMOS compatible	Large area of the MEMS switches	103.7	MEMS switches	4	2
[4]	MOSFET switched three layers MSI	Fully CMOS compatible	Low Q due to parsitics	187.5	Routing	Quasi-continuum	2
[5]	Metal shielding tuned using MEMS	High Q	Not CMOS compatible	77	Actuators and metal shield	4	1
[36]	A VO_2 switch connects a parallel inductor	Multiple states achievable by changing the temperature (for the VO_2 inductor)	Temperature $> 67°C$ required to maintain LRS. Large area required for the VO_2 switch.	32	In-line VO_2 switch, none for VO_2 loop inductor	≥ 3	Controlled by temperature

[1] The area overhead refers to the extra area required to implement the tunable capability of the inductor. The routing of control signals is not considered for area estimation.

peak Q and a lower SRF. The latter is due to the stacked structure, which adds parasitic capacitive coupling between the two spirals. Furthermore, MSIs provide increasingly higher inductance values per area. However, as the MSI is tuned by 'external' devices implemented in the top metal layer, a small area overhead is required.

The memristive–via switched tunable inductor provides increased opportunities for tunability, since the memristive–via can be placed in different locations to provide diverse values of inductance. Moreover, by controlling the compliance current, different values of R_{ON} can be achieved ($i.e.$, the width of the filament is changed). Thus, a quasi-continuum of inductances can be obtained. Added complexity is expected due to this scheme, as the controller must be smart enough to achieve the desired value. An outstanding advantage of this topology is the nonexistent area overhead, since memristive–vias are placed between the junction of the upper-layer and the cross-under conductors. Furthermore, no extra routing is required for control signals; the spiral itself is used for this purpose.

The number of states that can be added in an MSI is limited by the number of layers. An additional possible limitation might be due to a large parasitic capacitance between the layers, which would diminish the SRF to unacceptable low value. The memristive–via tuned inductor is limited by possible different achievable values of series resistance, if methodology (b) from Section III-C is to be implemented. Furthermore, these resistances could lead to an inadmissible drop of Q. A possible approach to adding more states is to combine both topologies, thus obtaining the advantages of both. For instance, a memristive–via can be added to each spiral in a MSI manner, achieving multiple levels ($i.e.$, six states for one memristive–via per spiral and a single RFMS SPDT). Increased maximum inductance and better Q

are expected when compared to a single layer memristive–via switched tunable inductor, with a slight reduction of the SRF.

It is worth mentioning that both Q and SRF are almost undisturbed by the RFMS; hence the inductors could be optimized. To further improve Q and SRF, several well-known RF-CMOS techniques can be introduced, $e.g.$, low-K dielectrics [30], Patterned Ground Shield (PGS) [31], substrate etching [32], or high-resistivity substrate [33]. Furthermore, some MEMS enhancing techniques could be tested, $e.g.$, 3D inductors [34] or suspended planar inductors [35].

B. Comparison to Other Technologies

Several variable inductors have been reported using both MEMS and transistors [2]–[5]. However, MEMS tunable inductors are far more popular than transistors due to their achievable high inductance, Q and SRF. As mentioned, the major drawbacks of MEMS technology are the significant area overhead, high biasing voltages, low switching speed, additional cost due to the complex fabrication process, and contact interface degradation.

Results of a comparison between different variable inductors reported in the literature and TIME are listed in Table V. In [4], an MSI switched by MOSFETs is reported. The main drawback of this device is its low Q due to parasitic losses of the transistor. In [5], a MEMS reported device is tuned by its metal shielding, which changes the magnetic field, thus varying its inductance. This device stands out for its high Q; however, it requires a large area, high bias voltage, and it is not fully CMOS compatible. Rais-Zadeh *et al*. present in [3] an inductor that varies by changing the mutual inductance between the main inductor and secondary inductors, which are switched by MEMS relays. A high Q inductor is achieved; however, extensive area is also required. In [36], Wang *et al.* present two tunable inductors. The first is topology is tuned by a VO_2 switch that connects or disconnects a second loop in parallel with the main loop inductor. The second topology implements the parallel loop inductor using VO_2 as the conductor ($i.e.$, without using any switch). A disavantage of VO_2 is that the temperature needs to be above 67°C to maintain the ON-state, which makes it less feasible for applications requiring a wider temperature range. Moreover, the switch requires a large area to achieve a low R_{ON} and the switching energy is significantly higher than for ECM memristive devices. TIME achieves high integration, with a smaller footprint than the listed devices, low-energy switching, and added non-volatility, which reduces the number of bias operations. Furthermore, results show that these devices provide good Q and high TR.

VI. Conclusion

In this paper, we present two TIME topologies, a memristive–via switched tunable inductor and a multi-layer stacked inductor tuned by RFMS SPDT. The two TIME topologies are designed and simulated using ADS, using a fitted model of RFMS in [11], and by simulating the structure of a hypothetical ECM memristive device based on reported fabricated devices. Results show that both topologies provide high tunability and Q, with a sufficiently high SRF for 5 GHz. Both Q and SRF can be improved by use of modern technology nodes or MEMS post-processing techniques.

Using memristive devices to reconfigure inductors reduces both the area overhead and the power consumption when compared to other technologies, still providing relatively high quality inductors. Therefore, the proposed TIMEs are promising key components for tunable multi-band RF circuits, and reconfigurable matching circuits. Furthermore, TIME straightforwardly leads to another possible application, tunable transformers, which have been employed in RF circuits for input and output matching. Future work will focus on optimization, full-wave simulations, fabrication and full characterization of the topologies.

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Nicolás Wainstein received the degree in electrical engineering from the Universidad de la República, Uruguay, in 2014. From 2014 to 2015, he was a Research and Teaching Assistant with the Institute of Physics and the Institute of Electrical Engineering, Universidad de la República.

He is currently pursuing the Ph.D. degree with the Andrew and Erna Viterbi Faculty of Electrical Engineering, Technion–Israel Institute of Technology. His current research interests include RF and analog circuits and systems using memristive devices.

Shahar Kvatinsky received the B.Sc. degree in computer engineering and applied physics and the M.B.A. degree from the Hebrew University of Jerusalem in 2009 and 2010, respectively, and the Ph.D. degree in electrical engineering from the Technion–Israel Institute of Technology in 2014. From 2006 to 2009, he was with Intel as a Circuit Designer and a Post-Doctoral Research Fellow with Stanford University from 2014 to 2015. He is currently an Assistant Professor with the Andrew and Erna Viterbi Faculty of Electrical Engineering, Technion–Israel Institute of Technology. His current research interests include circuits and architectures with emerging memory technologies and design of energy efficient architectures. He was a recipient of the 2015 IEEE Guillemin-Cauer Best Paper Award, the 2015 Best Paper of Computer Architecture Letters, a Viterbi Fellowship, a Jacobs Fellowship, an ERC Starting Grant, the 2017 Pazy Memorial Award, the 2014 and 2017 Hershel Rich Technion Innovation Awards, the 2013 Sanford Kaplan Prize for Creative Management in High Tech, the 2010 Benin Prize, and six Technion Excellence Teaching Awards. He is an Editor of the *Microelectronics Journal*.