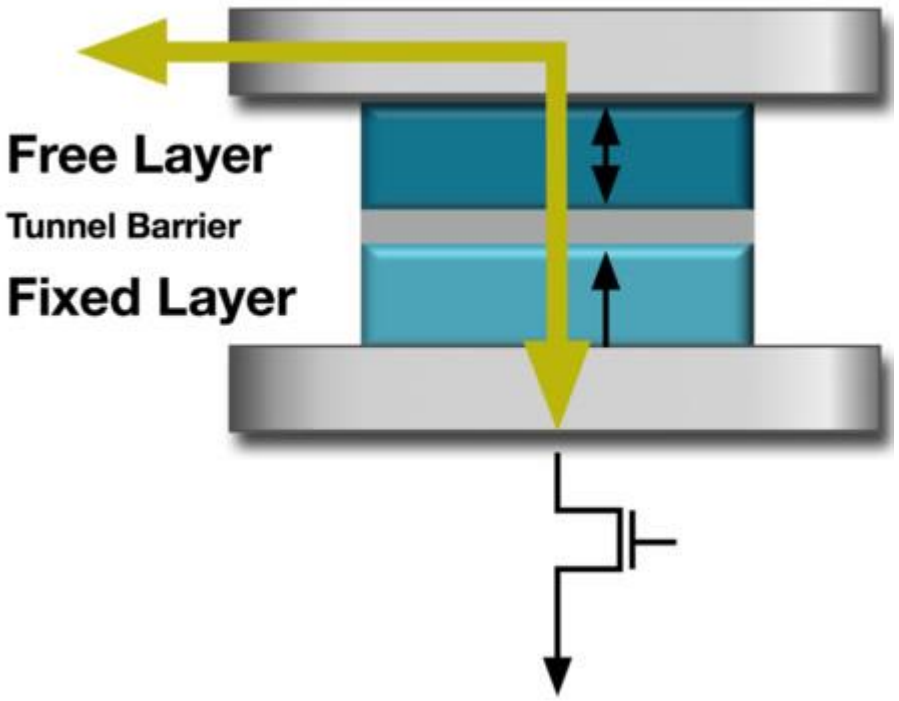
# Spin-torque Transfer MRAM controller for Risc-V

***Background:*** *Writes to a memory array by manipulating electron spin with a polarizing current, performs like DRAM but requires no refresh, significant reduction in switching energy compared to FS Toggle MRAM, highly scalable, enabling higher density memory products (sampling 1Gb in 2019), can interface with JEDEC DDR3 with minor modification, and is quite an attractive emerging memory. Let's use it!*




**Project Description:**

- Design a Memory I/F according Standard JESD79-3F, with exceptions and improvements as required to SST-MRAM state of art.
- Implement on FPGA
- Connect it to RISC-V core
- Test it and compare to DRAM DDR3

Perquisites: Computer organization and Design

Recommended: Lab1

Host: VLSI Lab

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