

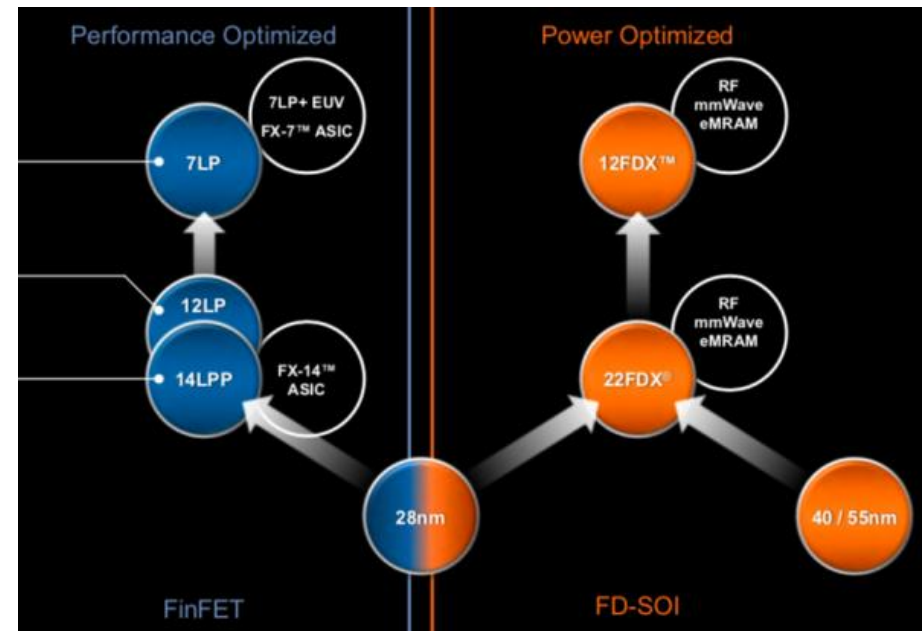
STT-MRAM Based Multistate Register

Background: . An STT-MRAM based multistate register will be designed, capable of storing multiple data bits within a single active register. The register compensates for the stochastic nature of STT-MRAM while enabling switching latencies compatible with modern microprocessor pipelines.

To do so we shall use 22FDX Global Foundries libraries.

Project Description:

- Read Paper
- Hands-on VLSI tools & Library integration
- Design Register
- Demonstrate



Prerequisites: Computer organization and Design

Recommended: Lab1

Host: VLSI Lab

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