

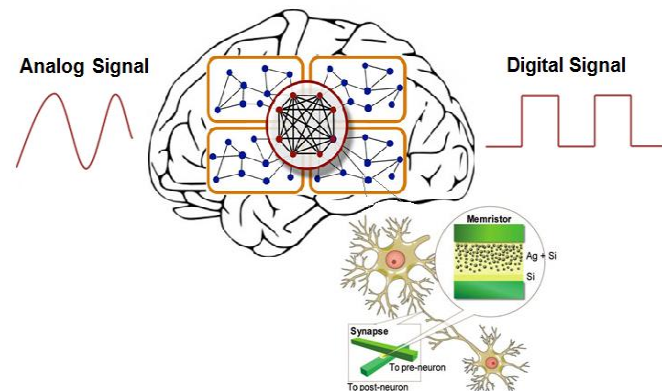
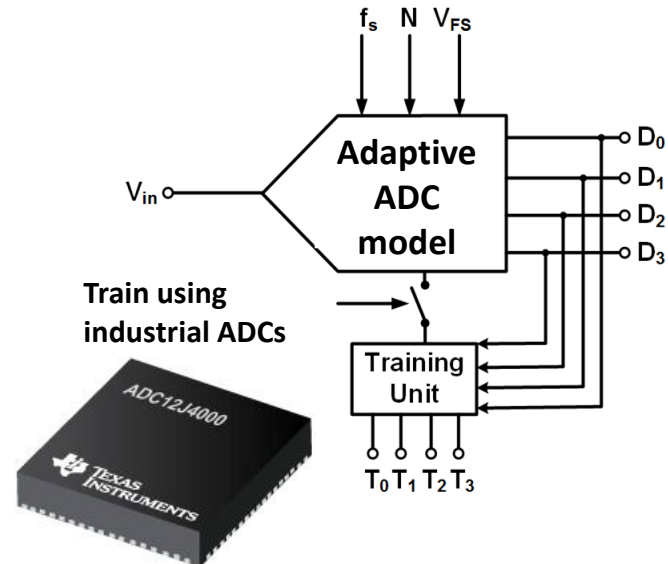
Taken

ASIC² Project: Adaptive Neural Network Model for Analog-to-Digital Converters (ADCs)

Background: The analog-to-digital converter (ADC) is a principal component in every data acquisition system. Unfortunately, modern ADCs trade off speed, power, and accuracy. In this project, novel neuro-inspired approaches will be used to design a smart ADC SPICE model that could be trained to fit for general purpose applications and a wide range of industrial ADC architectures. Motivated by artificial intelligent learning algorithms and neural network architectures, the proposed ADC model integrates emerging memristor technology with CMOS. In this project, students are required to model a trainable ADC with adaptive number of resolution bits, frequency and full-scale voltage using a memristive neural network that implements the online gradient descent algorithm. This supervised machine learning algorithm fits multiple application/architectures specifications: Flash, Pipelined, SAR, Sigma-delta. This model could be used as a generic SPICE model with high-accuracy, flexibility, scalability and reliability for any practical ADC.

Project Description:

- Theoretical study & comprehension of: ADCs, memristors, neural networks, and machine learning algorithms.
- SPICE modeling and simulations of the ADC using Verilog-a
- Lab measurements, evaluation & characterization of industrial ADCs: Flash, pipelined, SAR, and Sigma-delta.
- Fitting the ADC model to the measured ADCs by the training algorithm.
- Deliverables: verilog-a model, SPICE symbol, manual, measurements



Prerequisites: linear electric circuits, VLSI

Loai Danial, sloaidan@tx, VLSI Lab, ASIC2 Lab

data base, & real-time demonstration