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Understanding the influence of device, circuit and environmental variations on real processing in memristive memory using Memristor Aided Logic

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ABSTRACT

Memristors have gained increasing interest recently as emerging memory technologies. Their unique ability to perform logic operations within the memory makes them even more attractive. MAGIC NOR is one such logic gate that can be integrated within memristive memory cells, thus opening possibilities for real in-memory computing. This paper explores the integration of MAGIC NOR gates within large-scale memory crossbar arrays. We evaluate both analytically and numerically different non-ideality parameters that influence the logic gate performance. First, we investigate the effect of parasitic resistance and capacitance within the memory array. Then, process and device variations are considered and modeled, as well as environmental conditions such as temperature and power supply variations. These non-idealities are formulated in the form of process corners that enable designers to estimate the effect of variations on their design in worst case scenarios, similar to the manner in which such effects are estimated in CMOS-based VLSI design.

1. Introduction

Memristors are novel passive circuit elements [1,2] that are becoming increasingly common in the field of circuit design. The device has two terminals and effectively acts as a varying resistor. The momentary resistance (to which we refer as *memristance* for simplicity) is controlled by a state variable, whose derivative depends on the applied voltage/current across the device's terminals. Thus, the momentary resistance at any time is governed by prior operating conditions applied to the memristor. Being non-volatile, memristive technologies such as resistive random access memory (ReRAM), phase change memory (PCM) and spin-torque-transfer magnetoresistive RAM (STT-MRAM) make attractive candidates for replacing current memory technologies [3–5] across the memory hierarchy – from caches to storage. In addition to their use as memory elements, new uses for memristors in other fields, such as logic circuits [6–8], neuromorphic systems [9–13] and memory intensive architectures [14–16], are frequently proposed. The Memristor Aided Logic (MAGIC) [17] family is a set of stateful logic gates, wherein the logic state is stored in the form of resistance. The MAGIC NOR gate has been proposed for use as the basic logic element in 'logic within memory' [17–22] architectures, and is the main focus of this paper.

Recent literature have explored different aspects of MAGIC gates, including integration within a memristive crossbar array [19], architectural considerations to construct a memristive memory processing unit (mMPU) [23], limitations of parallelism and data distribution [24], and their fabrication [25–27]. This paper explores realistic issues that have not been explored yet and are essential for the realization of a working mMPU – the influence of disparities in performance due to fabrication process and environmental variations [28–32]. These variations include disparities in traditional circuit components that may be incurred by physical component dimensions (due to lithography or line edge roughness), chemical composition, voltage levels, and temperature. Similarly, the behavior of a memristor is subject to various deviations, somewhat different from the ones affecting traditional CMOS components. These disparities can be the result of process variations (*e.g.*, variations in size or ion concentration), environmental conditions (*e.g.*, ambient temperature) or circuit parameters (*e.g.*, variations in power supply) [33–36]. Previous work has explored the effect of process variations on the behavior of memristive memories [37]. Existing studies of the impact of variations on memristive logic [38] are limited to analyzing the effect of observed variations on gate performance rather than offering a methodology for circuit designers to evaluate their design.

In this paper, we study the effect of deviations in device behavior on the performance of a MAGIC NOR logic gate within a crossbar array.

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Our goal is to gain a more fundamental understanding on the behavior of these gates when subjected to deviations from ideal operating conditions. A sensitivity analysis is performed to better understand the desired device characteristics. The analysis is done based on a specific HfO_2 device, but the methodology is kept general and applies to various devices and technologies. The degree to which different parameters are varied is determined either by an absolute range, in cases where there is a clear physical justification in literature to setting such a range, or by a relative variation above and below the nominal value of the parameter, in cases where variations are strictly technology dependent. The results of this study may enable memristive logic circuit designs that are tolerant to changing environmental conditions and to process variations. These results may be applicable to other memristive logic families with the required adjustments. The two main contributions of this paper are:

- A study of the effect of various device, circuit and environment variations on the performance of MAGIC stateful logic gates operated within memory arrays.
- Formulation of variation impact in the form of corners, similar to those used in CMOS circuit design.

The rest of the paper is organized as follows. Section 2 contains necessary background regarding the operation of MAGIC logic gates. In section 3, our methodology and simulation setup are presented. Section 4 offers a description on the modeling of logic enabled memristive memories and the RRAM devices they contain. The performance impact of variations in parameters of the circuit, device and environment are respectively examined in sections 5, 6 and 7. These results are expressed in terms of corners for circuit design in section 8. Finally, conclusions are presented in section 9.

2. Memristor Aided Logic

Memristor Aided Logic (MAGIC) is a stateful logic technique, where the logical values '0' and '1' are represented, respectively, by high resistance (R_{OFF}, HRS) and low resistance (R_{ON}, LRS, $R_{OFF} \gg R_{ON}$). This family of gates consists of different Boolean functions such as NOT, AND, NAND, OR and NOR gates. The NOT, NAND and NOR gates are compatible with crossbar topology, which is a natural way of fabricating Metal-Insulator-Metal (MIM) memristive memory arrays [39]. The operation of all the gates in the family relies on a voltage divider between the inputs of the gate and its output. Prior to computation, the output memristor is initialized to LRS by means of applying an appropriate voltage pulse accross its terminals. Then, an operating voltage V_G is applied to the entire gate, and only if certain conditions are met, the voltage on the output will exceed a threshold (V_{th}) for switching between states. Thus, the operation of the gate can be viewed as a conditional write of the value '0' (RESET) to a device which was prewritten with the value '1' (SET). This means that all SET operations are performed directly by the peripheral circuits of the memory array, and only a RESET operation may be performed by the MAGIC NOR gate. The structure of a two input MAGIC NOR gate is shown in Fig. 1. When both inputs hold logic '0', their equivalent resistance is $R_{OFF}/2$. The operating voltage V_G is chosen so the voltage drop on the output memristor upholds

$$V_{OUT} = V_G \cdot \frac{R_{ON}}{R_{ON} + \frac{R_{OFF}}{2}} < V_{th,OFF}, \tag{1a}$$

where $V_{th,OFF}$ is the voltage level required to switch the device from LRS to HRS. Thus, the output memristor retains the value logic '1'. In all other input combinations, at least one of the input memristors holds logic '1' and the voltage drop on the output is therefore

$$V_{OUT} \geq \frac{V_G \cdot R_{ON}}{R_{ON} + R_{OFF} \parallel R_{ON}} > \frac{V_G}{2} > V_{th,OFF}, \tag{1b}$$

switching the output memristor to HRS, and realizing the NOR truth table.

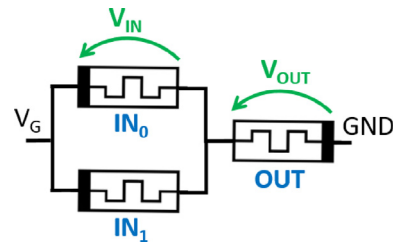

Fig. 1. Schematic of a two-input MAGIC NOR gate. IN_0 and IN_1 are the gate inputs, *OUT* is the gate output that is initialized to R_{ON}.

3. Methodology and simulation setup

The metrics used to evaluate the performance of the MAGIC NOR gate are, first, proper functionality, and second, the switching time of the output memristor. The MAGIC NOR gate design requires the output to be initialized to logic '1'; therefore, a switch in the output will occur if at least one of the inputs holds logic '1' before the NOR operation is applied. For measuring switching time, we consider a configuration in which the lowest voltage that should cause switching is applied to the output memristor. This 'worst case' scenario (*i.e.*, the slowest operation) in terms of the output switching time occurs when one input holds logic '1' and the other holds logic '0'. When a change of 50% in memristance is not observed within a time frame one order of magnitude longer than the typical switching time, we define this as a switching failure. For some of the parameters considered, a drift in the state of the input memristors may also be induced by variation. If the voltage applied to an input holding logic '0' exceeds a threshold voltage $V_{th,ON}$, the state of the input may drift toward R_{ON} and possibly change the result of the operation written to the output memristor. The state drift is addressed where applicable. Other metrics, such as dissipated power and area, are out of the scope of this paper.

To determine the impact of different types of variations on the switching ability and switching time of memristive logic gates, we performed dynamic analog circuit SPICE simulations using Cadence Virtuoso. Many of these simulations were preceded by exploratory circuit model analysis in MATLAB, using static equations derived from memristor and circuit rules. Using MATLAB to solve the differential equations for the circuit allows tuning the computationally demanding SPICE simulations to a simulation time step that produces results with fine resolution. This is done by using a range of simulation time steps, starting from a fine, femto-second scale, which is increased if the simulation does not converge. The simulation time can be iteratively increased thanks to the reduced computational complexity of simulating the modified circuit with MATLAB as compared to analog simulations in Virtuoso. Overall, the use of MATLAB allows us to find the switching time (under different variations) with limited accuracy, and then tune the timescale for the more accurate simulations in Virtuoso. The static and dynamic parameters of the memristor are based on physical measurements conducted in our lab on an HfO_2 resistive switch. Dynamic parameters are considered to be all parameters affecting device switching (*e.g.*, carrier mobility, threshold voltages, *etc.*); the other parameters (*e.g.*, physical size, HRS/LRS resistance values) are considered static.

4. Device and circuit models

Analog simulations employ the VTEAM model, a generic memristor model introduced by Kvatinsky et al. [40] which allows emulating the behavior of a wide range of devices by tuning the model parameters. The principal equations of the model are

$$I(t) = \left[R_{ON} + \frac{R_{OFF} - R_{ON}}{w_{OFF} - w_{ON}} \cdot (w - w_{ON})\right]^{-1} \cdot V(t), \tag{2a}$$

$$\frac{dw(t)}{dt} = \begin{cases} k_{OFF}\left(\frac{V(t)}{V_{th,OFF}} - 1\right)^{\alpha_{OFF}} & 0 < V_{th,OFF} < V(t) \\ 0 & V_{th,ON} < V(t) < V_{th,OFF} \\ k_{ON}\left(\frac{V(t)}{V_{th,ON}} - 1\right)^{\alpha_{ON}} & V(t) < V_{th,ON} < 0 \end{cases} \tag{2b}$$

where $\alpha_{ON/OFF}$ and $k_{ON/OFF}$ are memristor parameters representing, respectively, the degree of non-linearity in the switching process and the switching speed (governed by ion mobility). w is the state variable used by the model, and w_{OFF} and w_{ON} are, respectively, the minimal and maximal values it can attain. The model is fitted to measured experimental data using an automated fitting tool which is run on the device's I–V measurements [41]. Using the VTEAM model allows to capture the behavior of the specific device used, while allowing to tune various parameters which relate to different possible variations, thus making it adequate for our analysis.

Full schematic of a MAGIC NOR gate within a memristive crossbar array and its equivalent simplified schematic are shown in Fig. 2. The differential resistances in Fig. 2(a) are the resistances of the wires connecting the memristors within the crossbar. In Fig. 2(b) these resistances are lumped to represent the resistance values connected to each of the circuit's active nodes. The resistors connected to the voltage source (r_s), common node (r_{wl}) and separate nodes (r_{bl}) represent, respectively, source non-linearity, wordline resistance and bitline resistance. The method for accumulating these resistances is discussed in Sections 5.2 and 5.3. Additionally, a lumped capacitance (C) is added, connected to the common node, representing the cumulative parasitic capacitance in the circuit as discussed in Section 5.1.

Developing the circuit equations according to Kirchhoff's laws for the schematic in Fig. 2(b), when considering the memristor model in (2a), we get

$$\frac{dVc}{dt} = \frac{1}{C \cdot R_{par}} \cdot \left[V_G + V_{OUT} - V_{OUT} \cdot \frac{R_{par} + r_{wl,OUT} + R_{ON}(w - w_{ON})}{R_{ON} + R_w(w - w_{ON})} \right], \tag{3a}$$

$$V_{OUT} = \frac{V_C}{1 + \frac{r_{wl,OUT} + r_{bl}}{R_{ON} + R_w(w - w_{ON})}}, \tag{3b}$$

$$\frac{dw}{dt} = k_{OFF}\left(\frac{V_{OUT}}{V_{th,OFF}} - 1\right)^{\alpha_{OFF}}, \tag{3c}$$

where

$$R_{par} = (R_{IN_0} + r_{wl,IN_0} + r_{bl}) \| (R_{IN_1} + r_{wl,IN_1} + r_{bl}), \tag{3d}$$

$$R_w = \frac{R_{OFF} - R_{ON}}{w_{OFF} - w_{ON}}. \tag{3e}$$

R_{par} is the equivalent resistance of the two input memristors and their adjacent wires. For the static MATLAB analysis, the states of the input memristors IN_0 and IN_1 are assumed not to change; thus they are treated as two resistors with values R_{OFF} and R_{ON}, respectively.

Baseline configuration: The values for the parameters used in the simulations are listed in Table 1. The model parameters are chosen to match the behavior of the HfO_2 device with Ti/TiN electrodes that was measured in our lab, and is described in detail in Ref. [42]. The device is fabricated in 90 nm process technology, with physical dimensions of 0.09 μm × 0.09 μm. The switching time of the device is 50ns. The listed circuit parameters represent the ideal case, in which all the parasitics are zero. The resulting ideal output switching time for a MAGIC NOR gate is 76.4ns.

The following sections describe the parameters that are varied to establish the memristive logic *Corners*, as well as the results of their variations. As customary in CMOS back end of line (CMOS BEOL) corner formulation [43], we refer to PVT (Process, Voltage, Temperature) corners. Voltage and temperature are considered as environmental parameters. Process parameters, which in CMOS BEOL refer to fabrication physical dimensions, are considered here to be parameters affected by the fabrication process: either parameters of the memristive devices or parameters of the rest of the circuit.

5. Circuit parameters

In this section, we explore different possible circuit parameter changes and their effect on the switching time of a MAGIC NOR gate operated within a memristive array. The explored parameters are parasitic capacitance (Section 5.1), wordline and bitline resistances (Sections 5.2 and 5.3, respectively), and the number of inputs of the gate (Section 5.4).

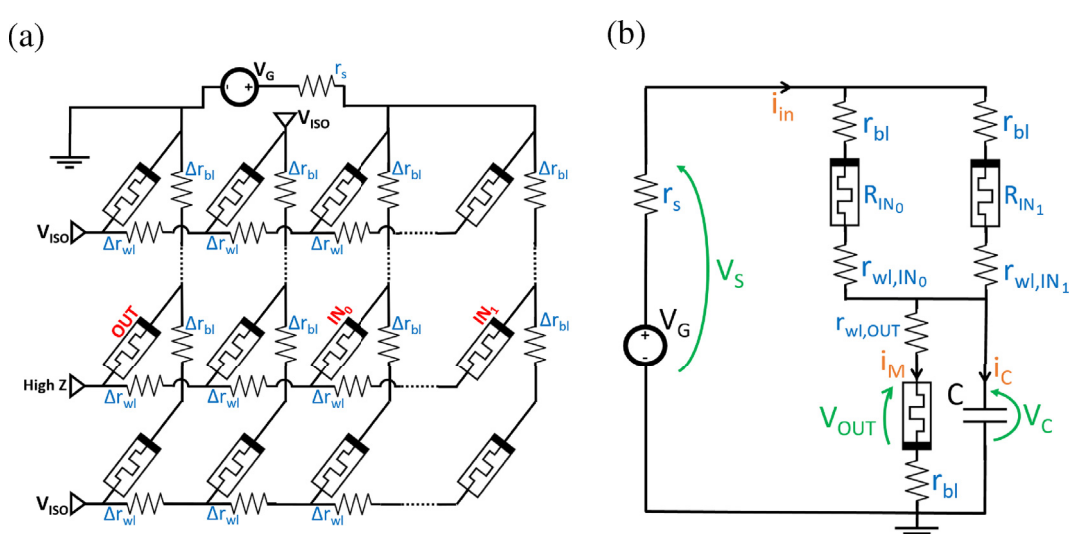

Fig. 2. Schematics of the simulated MAGIC NOR circuit within a memristive crossbar array. (a) The full crossbar view demonstrates the physical connection between all the devices in a crossbar during the operation of a MAGIC NOR gate. (b) An equivalent reduced circuit shows only the devices participating in the NOR gate.

Table 1
Memristor and circuit parameter values.

Parameter		Description	Typical Value
VTEAM Memristor Model Parameters	R_{ON}	LRS Resistance	7kΩ
	R_{OFF}	HRS Resistance	173.8 $k\Omega$
	k_{ON}	Ion Mobility in SET	198.72 mm/sec
	k_{OFF}	Ion Mobility in RESET	28.921 nm/sec
	D	Filament Physical Length	10 nm
Circuit Parameters	r_{bl}	Bitline Serial Resistance	0 Ω
	r_{wl}	Wordline Serial Resistance	0 Ω
	C	Common Node Capacitance	0 F
	r_s	Voltage Source Resistance	0 Ω
	V_G	Voltage Source Magnitude	1.4 V
Fitting Parameters (Unchanged)	$\alpha_{ON(OFF)}$	Non-linearity Factor	1 (2)
	$V_{th,ON(OFF)}$	Switching Threshold Voltage	0.45 (−0.7) V
	$w_{ON(OFF)}$	State Variable Extrema	10^{-8} (0)

5.1. Parasitic capacitance

The crossbar array structure, in which MAGIC NOR gates are likely to be manufactured, has parasitic wire capacitance, formed between the metal lines and memristor terminal electrodes to the bulk and to adjacent metal lines [44,45]. This capacitance is increased with wire width and memristor size. The capacitance of wires directly connected to the ground is neglected because the voltage of these wires is determined solely by the connected source. The input nodes are connected to a voltage source, which produces a voltage pulse. However, assuming that the sources have a sufficiently strong driving force, the capacitance of these nodes will add a constant delay to the operation of the gate and is hence ignored as well. We also neglect internal capacitance between the memristor electrodes. Hence, we consider only added capacitance on the common node, which is modeled as a capacitor connected from this node to the ground. The added capacitance value may vary in a range of many orders of magnitude depending on the materials used and their physical dimensions and geometry. Therefore, simulations are conducted with a range of capacitance values, although the higher values may be irrelevant for standard process technologies. The results of the Virtuoso and MATLAB simulations, as well as the calculation of the time constant $\tau = R_{eq}C + t_0$, are shown in Fig. 3, where t_0 is the switching time of 76.4ns observed without any added capacitance ($C = 0$). τ is considered as a lower bound on the switching time as it does not capture the dynamic behavior of the circuit (resistive switching induced by a changing voltage).

Our results show consistency among the different models for most of the low capacitance values. The switching time for low capacitance is governed by the time to charge the capacitor. At first, for the lowest capacitance values evaluated, this time is negligible compared to the switching time of the memristor. For medium capacitance values (1 pF to 100 nF), most of the switching time is spent on charging the capacitor to a level sufficient for switching the output. High capacitance values (higher than 100 nF) demonstrate a slightly lower switching time in Virtuoso simulations than in the other two methods of evaluation. The reason for this difference is that the SPICE simulations consider two phenomena that the analytic model and MATLAB do not consider. First, the output switching may begin when the capacitor is not yet fully charged. Second, there is a state drift of one input from '0' to '1' for these capacitance values (see inset in Fig. 3). The input drift causes higher voltage drop on the output memristor, thus speeding up the switching. However, this renders the logic gate unusable for the conditions at hand. Overall, an added capacitance between the common node of a gate and ground increases the switching time proportionally to the capacitance value. Capacitance between two adjacent nodes in a crossbar is reported to be 0.046 fF [46], which is in the lower end of the presented scale. However, a similar analysis done for different devices and circuit topologies may observe the effect of capacitance change starting from a much lower degree of variation. In our case, the maximal common node capacitance for a wordline containing thousands of cells amounts to a few hundred fF and an increase of up to a 10x in the switching time. This is tolerable if a low switching time is not the critical requirement of the desired logic. However, if the capacitance rises above a point that makes charging it slower than switching the inputs from R_{OFF} to R_{ON}, the gate will fail due to input state drift considerations. This behavior is highly dependent on the device parameters, such as threshold voltages and carrier mobility.

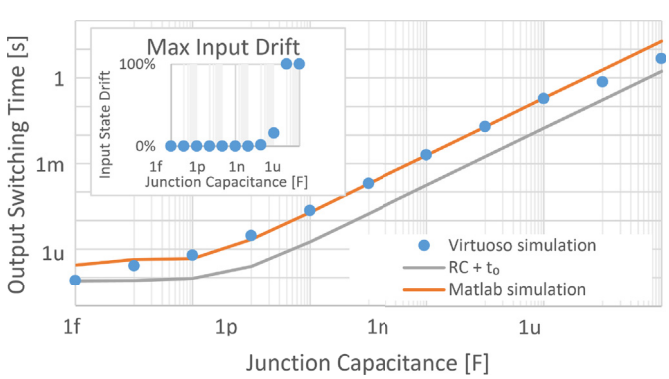

Fig. 3. Switching time for different values of junction capacitance. Results are presented for Virtuoso simulations (blue dots), analytic model of capacitor charging through a constant resistor (gray) considered as a lower bound, and MATLAB simulations (orange). The inset presents the percentage of maximal input state drift. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

5.2. Wordline resistance

To evaluate the effect of added wordline resistance, we examine the NOR gate from a crossbar design perspective, as illustrated in Fig. 4. The memristors of the gate can be arranged in any order within a wordline (*i.e.*, any permutation of the triad IN_0, IN_1, and OUT). Assume a constant resistance per unit length of wire, setting one resistor to 0 Ω and the others to higher values allows us to simulate the effect of the relative physical distance between the memristors within a gate. The resistance for a single segment of wire connecting two adjacent columns is in the order of 1 Ω [47], and may be even lower for wires with a large cross-cut. To simulate the fact that any arbitrary order of memristors within a wordline can perform a MAGIC NOR gate, the resistor connected to the middle memristor in the gate is set to be 0 Ω and the resistors connected to the other two memristors are set to different resistance values. Simulations are conducted with wire resistances ranging from 1 $m\Omega$ to 10 $k\Omega$, covering a crossbar size of up to $10k \times 10k$ cells.

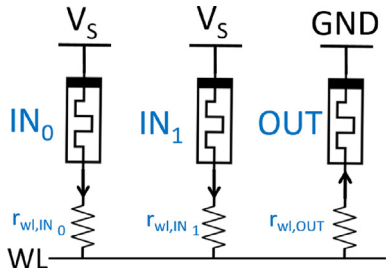

Fig. 4. Crossbar equivalent schematic of a MAGIC NOR gate for wordline resistance analysis. Any permutation in the order of the three memristors along the wordline is permitted when executing a MAGIC NOR operation.

For proper behavior of a MAGIC NOR gate, the following conditions must be maintained [17]:

$$\frac{V_G}{V_{th,OFF}} > \frac{R_{OFF}(IN_0)\|R_{ON}(IN_1) + R_{ON}(OUT)}{R_{ON}(OUT)}, \tag{4a}$$

$$\frac{V_G}{V_{th,OFF}} < \frac{R_{OFF}(IN_0)\|R_{OFF}(IN_1) + R_{ON}(OUT)}{R_{ON}(OUT)}, \tag{4b}$$

$$\frac{V_G}{V_{th,ON}} < \frac{R_{OFF}(IN_0)\|R_{OFF}(IN_1) + R_{ON}(OUT)}{R_{OFF}(IN_0)\|R_{OFF}(IN_1)}. \tag{4c}$$

If the condition in (4c) holds for the baseline values given in Table 1, it will hold also with additional resistance connected to the memristors. Thus, the two remaining constraints limit V_G. When (4a) is broken, no switching will occur even when it is expected. When (4b) is broken, at least one of the inputs may not retain its value during the operation. These constraints impose bounds on the value of the operating voltage V_G. Fig. 5 in this section, and Figs. 6, 8 and 15 in the following sections,

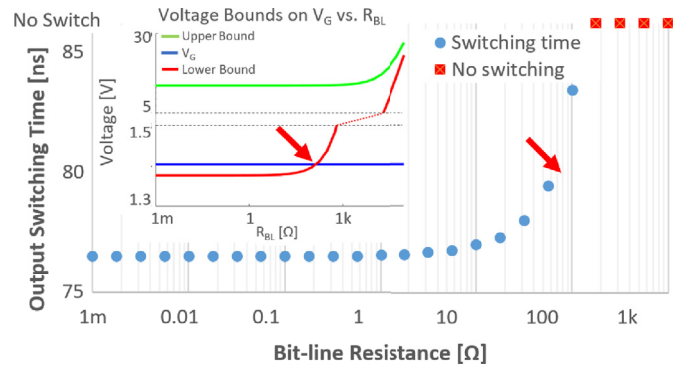

Fig. 6. Influence of bitline resistance on MAGIC NOR operation. The output switching delay is measured using SPICE simulations, when one input is 1 and the other is 0. Red squares indicate no switching is observed. Theoretic bounds on operation voltage as determined by (4a) considering bitline resistance are shown in the inset. The red arrows mark the point where the lower bound rises above the operating voltage, causing a failure in the operation of the gate. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

show these constraints for different parameter values. In these figures, a gate is assumed to function properly as long as the operating voltage is situated between the upper and lower bounds, whose value may change as a result of parameter variations. If the upper bound drops below the operating voltage, undesired switching of the output may occur, and if the lower bound rises above the operating voltage, the output may not switch when it is expected to. Thus, whenever a variation in any of the parameters causes the operating voltage of the gate to be located

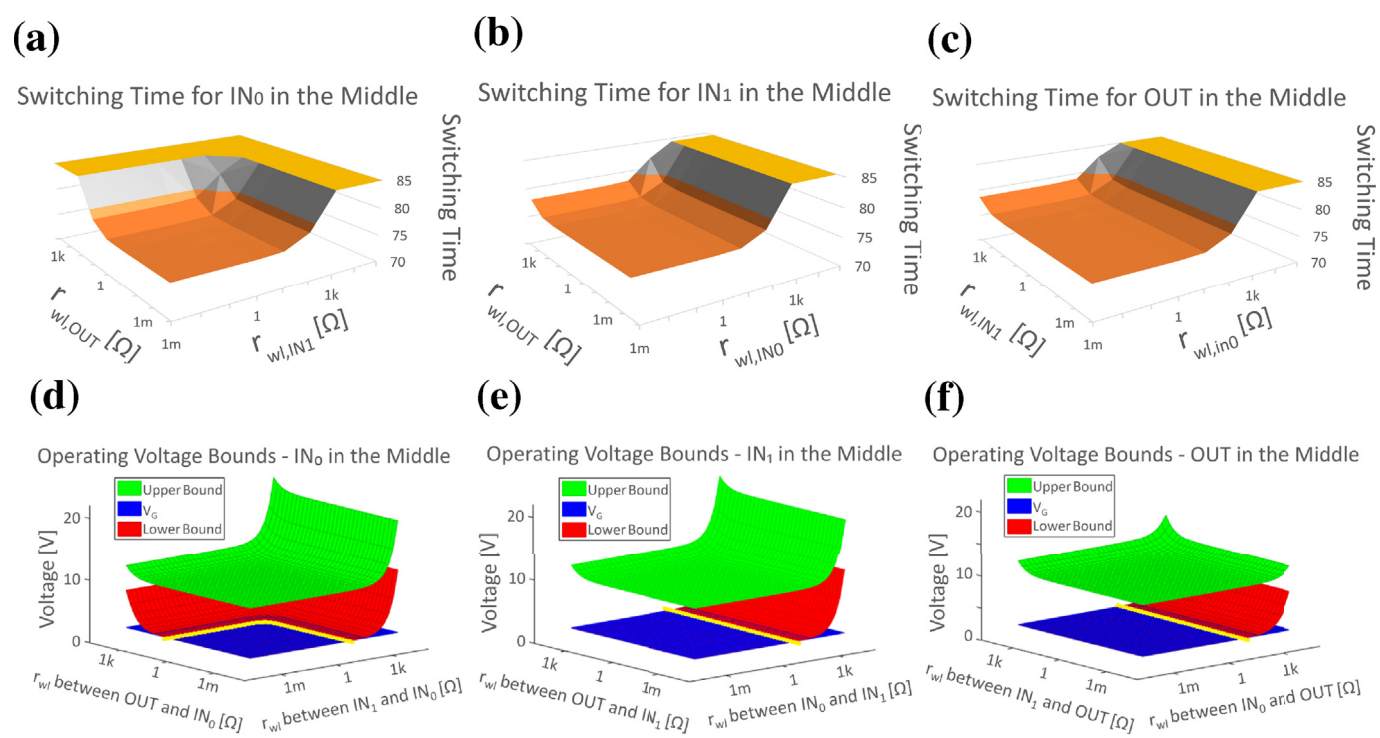

Fig. 5. Influence of wordline resistance on the MAGIC NOR operation. The gate delay is the output memristor switching time and it increases for larger distance between the memristors in all ordering of memristor in which (a) IN_0, (b) IN_1 and (c) OUT are in the middle. The saturated yellow region represents wordline resistances for which no switching occurs. (d–f) The constraints imposed on the gate operating voltage V_G for the different memristor ordering for different wordline resistance (proportional to the distance between the memristors). In each graph, the yellow line marks the place where the lower bound rises above the operating voltage, which results in a failure to switch the output. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

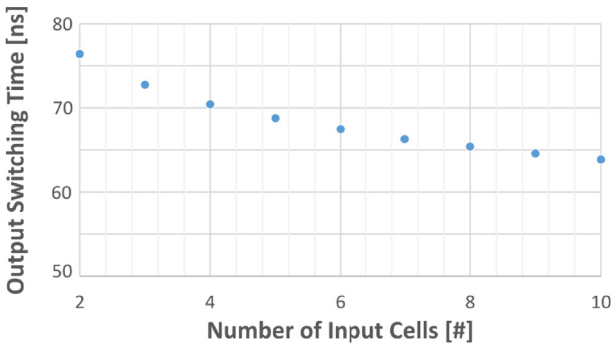

Fig. 7. MAGIC NOR output switching time for different number of inputs.

outside the bounds set by these conditions, we expect a failure in the gate's operation.

Simulation results and a visualization of the constraints for different wordline resistance are shown in Fig. 5. The results indicate that a large physical distance (*i.e.*, a distance which results in a wire resistance greater than R_{ON}) between the output memristor and an input memristor holding '1' will cause the gate to fail. Adding a large resistance to the wire connecting to the output memristor will cause more of the voltage to drop on that branch of the circuit, but most of it will not drop across the memristor and there will be no switching. Adding the resistance to the wire connected to the input with R_{ON} will raise the equivalent resistance of both input memristors until, for a sufficiently high added resistance, the circuit will perform as if both inputs were in the '0' state. The branch with the memristor holding '0' is not affected by added resistance because the voltage drop across the inputs is primarily determined by the memristor with lower resistance. Therefore, the maximal crossbar size that will support logic operations for any arbitrary location is determined by the LRS resistance of the individual cells and by the differential wire resistance between two adjacent nodes. For example, with the parameters used in this analysis, $R_{ON} = 7\ k\Omega$ and a differential wire resistance of 1 Ω, the maximum crossbar size is 7000 × 7000 cells, yielding a capacity of 49*Mbits*. The limitation imposed by process variations should, of course, be considered alongside any other limitations arising from the crossbar structure (*e.g.,* sneak paths). Therefore, the total crossbar size may be further limited [48,49].

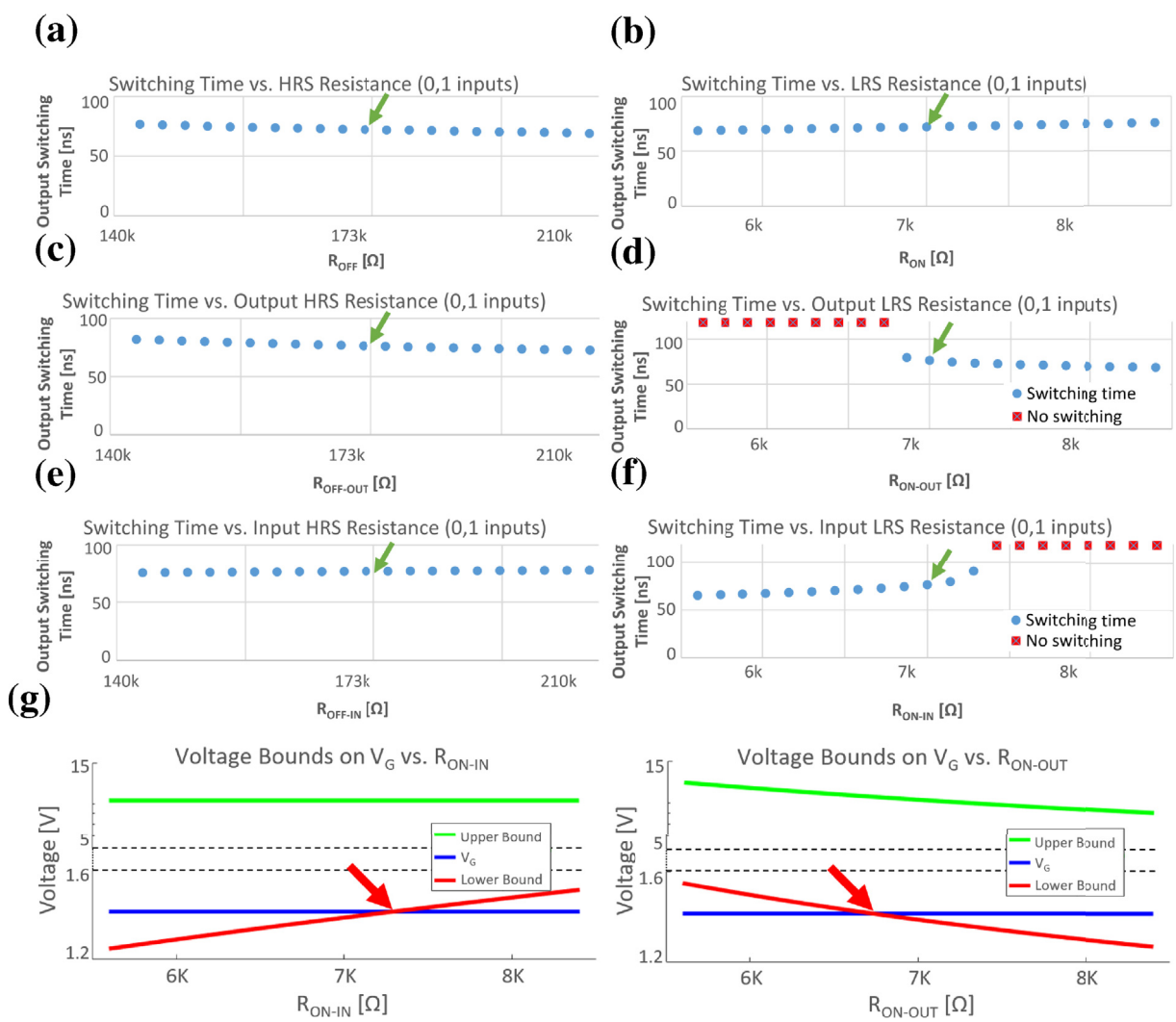

Fig. 8. Influence of different memristor resistances on the MAGIC NOR output switching time for input combination of 0, 1 or 1, 0. Green arrows mark the baseline configuration. Global variations in the (a) HRS and (b) LRS have a moderate effect on the switching time. Variations in the HRS of only the (c) output or (e) inputs also have a minor effect. Small variations in the LRS of only the (d) output or (f) inputs may cause a failure in gate operation, which is marked by red squares. Marked on the (g) voltage bounds from (4a), red arrows represent the point at which the lower bound increases above the operating voltage corresponding to switching failure. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

5.3. Bitline resistance

The bitline resistance is identical across all the memristors in a single gate. This is because the MAGIC NOR operation is performed on three memristors in a single row. Serially adding resistance in the order of R_{ON} or higher to all of the memristors in the gate disrupts the gate operation. Considering that the operating voltage is chosen to be as low as possible, any significant resistance increase to the output memristor will cause the gate to fail. Simulation results and theoretic bounds derived from (4) for bitline resistance variations ranging from 1 $m\Omega$ to 10 $k\Omega$ (corresponding to either an entire word line or an entire bit line of the crossbar, as described in Section 5.2) are shown in Fig. 6. Note that when performing a MAGIC NOR operation across columns instead of rows [19], the effect of wordline resistance (subsection 5.2) should be determined on bit lines (subsection 5.3) and the effect of bitline resistance should be determined on word lines.

5.4. Number of inputs

A MAGIC NOR gate may have more than two inputs [17]. Any additional input values are stored prior to the computation as resistance values of memristors connected in parallel to the two original input memristors. Fig. 7 shows the effect of increasing the number of inputs on the switching time for the worst case. The worst case occurs when all input values are logic '0' except for a single input which holds the value logic '1'. Simulation of additional inputs is done by adding a varying number of input branches identical to those seen in Fig. 2, in parallel to the two existing inputs. The added inputs reduce the equivalent resistance of all input memristors; hence, more of the applied voltage falls on the output memristor, accelerating the switching. This remains true also for the non-worst cases where any added input with value logic '1' increases the voltage drop on the output memristor even further. However, for the case of all inputs holding the value logic '0', the increased voltage on the output memristor may cause undesired switching. This failure may be avoided by limiting the number of inputs, upholding a constraint on the operating voltage extending (1a) to the case of multi-input MAGIC gates:

$$V_{OUT} = V_G \cdot \frac{R_{ON}}{R_{ON} + \frac{R_{OFF}}{\chi}} < V_{th,OFF}, \tag{5}$$

where χ is the number of input memristors.

6. Memristor parameters

In this section, the effects of device parameters on the switching time of a MAGIC NOR gate are explored. The memristor parameters are HRS and LRS (Section 6.1), fabrication process physical dimensions (Section 6.2), ion concentration resulting from fabrication and from the electroforming process (Section 6.3), and the threshold voltage for switching between resistive states (Section 6.4).

6.1. Memristor resistance

The extreme resistances of a memristor are those found at the edges of the range of allowed resistance values for a given device, namely R_{ON} and R_{OFF}. These resistances may be affected by variations in the manufacturing process [33], as discussed in subsection 6.2. While the effect of process variations on resistance is similar for both HRS and LRS resistances, the initial and final resistance states of the devices may also be affected by cycle-to-cycle variations (even under the same SET or RESET pulsing conditions). Therefore, it is imperative to examine the effect of changes on each of these resistances separately. The results for changing R_{ON} and R_{OFF} by ±20% globally and separately for the inputs and output are shown in Fig. 8, along with the relevant constraints from (4a). Linearly changing R_{ON} and R_{OFF} values globally, or changing R_{OFF} for the inputs and output separately, produces a predictable linear dependency between the switching time and the resistance. This dependency causes a change of up to ±7% in the switching time for a change of ±20% in the resistance. Only a large change in values (in the order of R_{OFF}) will cause a failure in gate operation. However, Fig. 8(d) and (f) demonstrate that an uncorrelated change in R_{ON} in the inputs and output yields interesting results. Even a small change in the value of R_{ON} can cause the gate not to switch, and the direction thereof is opposite when occurring in an input memristor or in the output memristor. Thus, if a process is prone to variations that are inconsistent between devices, higher operating voltages will likely be required to increase the noise margin necessary to differentiate between input states. It should also be noted that, depending on the technology used, some devices are reported to have cycle-to-cycle resistance variations that may be orders of magnitude larger than the typical resistance values. These devices are incompatible for use with the memristive logic considered here, as it requires a minimal amount of certainty regarding the resistance states of the memristors.

6.2. Process size variations

Process variations may affect the physical size of the memristor [34,50,51]. For memristors fabricated as an insulator in a junction between metal wires (namely, MIM structure), these variations may be categorized as those affecting the cross-section area of the junction S, and those affecting junction height h. These are represented by θ_S and θ_h respectively, where

$$\theta_S = \frac{S_{Junction}}{S_{typical}}, \tag{6a}$$

$$\theta_h = \frac{h_{Junction}}{h_{typical}}. \tag{6b}$$

The area of the junction affects the range of resistance values a device can attain in an inverse proportional manner [34]. For a filamentary switching mechanism, the resistance primarily depends on the formation of a single filament (winner takes all), but our worst case analysis takes variations in junction area into account as well. The junction height proportionally affects both the resistances and the total device length [34]. The analyzed effect of junction size variations on resistance and device length, taken from Ref. [34], are reflected in our simulations by changing the values of D, R_{OFFS} and R_{ON}. Results are shown in Fig. 9 for geometry variation of up to 20%. The effect on the switching time due to decreasing θ_S is marginally higher than that of increasing θ_h. On the other hand, increasing θ_S has a slightly lower effect than decreasing θ_h by the same ratio. This is expected because an inverse proportional influence is more effective when decreasing the value and less so when increasing it. The overall switching time changes in the range of −31% to +46% when changing both parameters by ±20%.

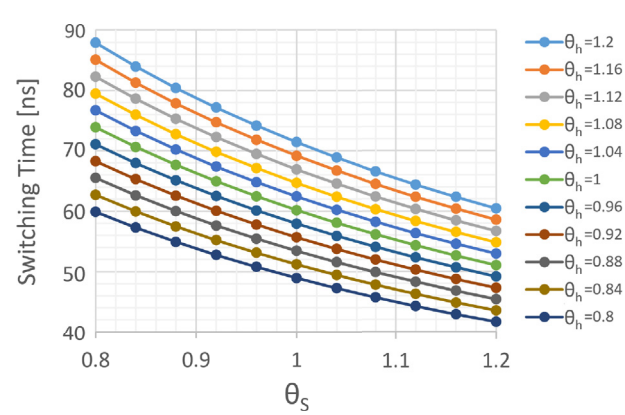

Fig. 9. Influence of process size variations on MAGIC NOR switching time for different junction cross-section area θ_S and height θ_h.

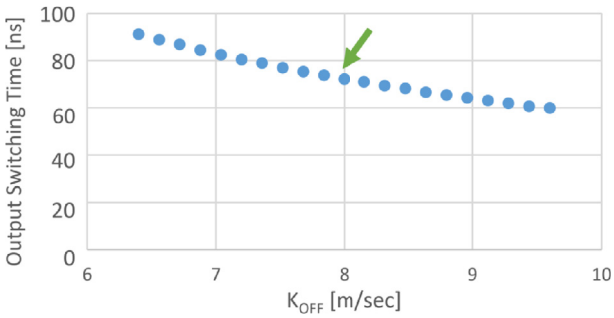

Fig. 10. Influence of variations in ion mobility as represented by the switching coefficient k_{OFF}. The green arrow marks the value of the baseline configuration. The output switching time is determined for input cases of 0,1 and 1,0. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

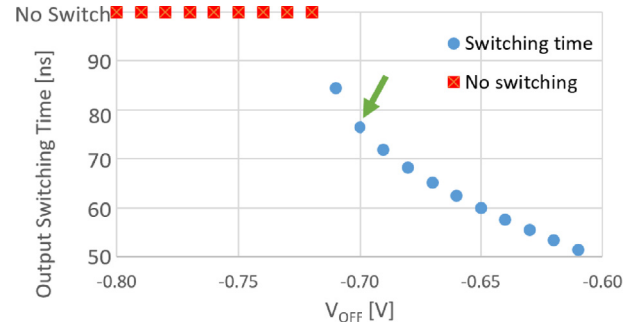

Fig. 11. Influence of variations in threshold voltage V_{OFF}. The green arrow marks the value of the baseline configuration. The output switching time is determined for input case of 0,1 and 1,0 and cases where no switching is observed are marked with red squares. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

6.3. Ion concentration

Another process variation that may occur in HfO_2 memristors is in the concentration of oxygen ions inserted into the oxide while forming the device [33]. This will affect the rate at which the device changes its state, in addition to the extreme resistances discussed in the previous subsection. The behavior is modeled by the parameters k_{ON} and k_{OFF} in the VTEAM model. In the case of a NOR gate, the only desired switching is of the output memristor from LRS to HRS, so only k_{OFF} is expected to have any effect on switching time. Fig. 10 indeed shows that changing the value of k_{OFF} by $\pm 20\%$ has an inverse linear correlation to the switching time. This variation is shown to affect the switching time considerably. However, it cannot cause the gate to fail because it only affects the change rate of the state variable, and not the voltage division across the input and output memristors.

6.4. Switching threshold voltage

The threshold voltage between the different resistance states a device can hold has a critical impact on the performance of a MAGIC gate. This can be seen directly from the dependence of (1) on the threshold voltage V_{OFF}. Variance in the threshold voltages of a device can be the result of various causes, including deviations in physical size, ion concentration, chemical composition. The threshold voltage V_{OFF} determines the conditions under which the output memristor will change its state from logic $'1'$ to $'0'$. A higher magnitude of V_{OFF} is expected to make the gate operate slower, until at some point it will fail switching due to an insufficient voltage falling on the output memristor. A lower V_{OFF} will make the gate operate faster, but at some low value the voltage on the output memristor will cause it to switch even when the inputs are in the (0,0) state, which constitutes a logic failure. However, with the expected high R_{OFF}/R_{ON} ratio, this failure will require a very low magnitude of V_{OFF}. On the other hand, V_{ON} determines the conditions in which we may expect to witness a drift in the state of the inputs. A value of V_{ON} that is too low will cause the relatively low voltage that falls on the inputs when at least one of them hold logic $'1'$ to switch the input to logic $'0'$. For our device, sweeping the magnitude of V_{OFF} in the range of ± 0.1 V(15%) from the baseline value causes the behavior shown in Fig. 11 which is consistent with our analysis, although not reaching the point at which unwanted switching is observed. The same variation applied to V_{ON} does not reach any substantial drift in the input values throughout the operation of the gate. However, as the behavior depends significantly on the gate's operation principle and the R_{OFF}/R_{ON} and V_{OFF}/V_{ON} ratios, this is by no means the general case. Each designer of stateful logic gates needs to perform a similar analysis that suits their specific logic gate and device properties.

7. Environmental parameters

In this section, the effects of varying ambient temperature (Section 7.1) and voltage source non-ideality (Section 7.2) are examined.

7.1. Temperature

Several studies have been conducted on the effect of ambient temperature on resistive switching behavior in HfO_2 devices [35,36,52], as well as on other memristive materials. This section relies on the theory in Refs. [53,54] and experimental results in Refs. [35,52]. These studies indicate that HRS resistance decreases and LRS resistance increases when temperature is higher. The HRS dependence is greater than that of the LRS. Therefore, increasing the temperature results in a reduction of the R_{OFF}/R_{ON} ratio. These results are also confirmed for the device used in this study in the temperature range $233K$–$398K$ ($-40°C$–$125°C$), as shown in Fig. 12. It is also reported that switching dynamics depend on temperature via a change in the mobility of the oxygen vacancies that serve as charge carriers. This dependency is described by the following Arrhenius-like equation:

$$\mu \propto \frac{1}{K_B \cdot T} e^{-\frac{E_A}{K_B \cdot T}}, \tag{7}$$

where K_B is the Boltzmann constant, T is the temperature in Kelvin and E_A is the activation energy of the resistive switching material lowered by the applied electric field. In the case shown here, the activation energy is 1.6 V [42]. A temperature fitting of the parameter K_{OFF}, which expresses the charge carrier mobility in the VTEAM model, is

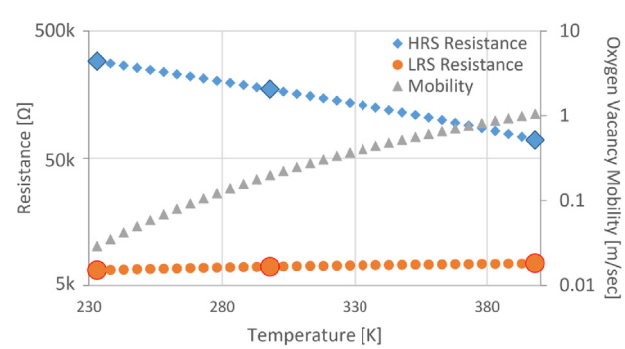

Fig. 12. Resistance and charge carrier mobility variation as a function of the temperature. Resistance values were experimentally measured for room ($298K$) and extreme ($233K$, $398K$) temperatures, and interpolated according to (7). The measured values are denoted by large markers, whereas the smaller markers represent interpolated values.

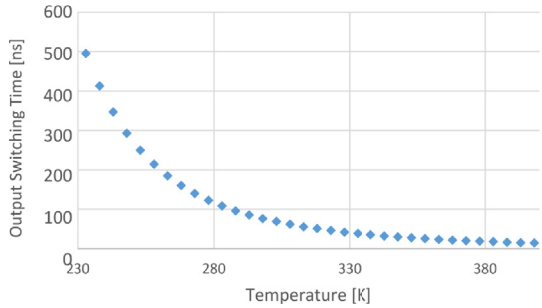

Fig. 13. Influence of temperature on the output switching time.

also shown in Fig. 12. Note that the change in K_{OFF} due to temperature variations is considered independently from the change as a result of variance in ion concentration discussed in subsection 6.3.

Varying temperature has two opposite consequences (changes in R_{OFF}/R_{ON} ratio and in charge carrier mobility) that influence the switching characteristics of a MAGIC NOR gate. Hence, they need to be considered concurrently in order to determine the overall effect of temperature. For the device considered in this paper, the change in resistance values is much less dominant than the change in mobility, and as seen in Fig. 13, the switching time of the output is lower for higher temperatures. However, this cannot be considered as the general case, and an analysis with appropriate parameters must be conducted for other memristive devices. In our analysis, the changes in switching time did not amount to a failure of the gate within the desired temperature range. However, it is observed that switching time is almost one order of magnitude higher in the worst case than at room temperature, which leads to the conclusion that different devices may fail.

7.2. Voltage source non-ideality and variations

Supply voltage source may have variations in the voltage magnitude. Applying a voltage above (below) the boundaries determined for proper behavior of the logic gate [17] will cause a logic failure by switching for unwanted input combinations (not switching for wanted combinations). Furthermore, less extreme variations also have an effect on the behavior of the logic gate. Lowering (raising) the operating voltage by 10% results in an increase of up to 31% (decrease of up to 27%) in switching time, as shown in Fig. 14. Parameters for the simulated gate are chosen with minimal operating voltage for the case of (0,1) inputs. Therefore, even a slight drop in the supply voltage will cause the gate to fail in this case. For the case of (1,1) inputs, the range of allowed voltages is wider due to a lower equivalent input resistance, causing the gate switching time to increase when reducing the voltage, until reaching failure at 1.1 *V*. The voltage needed to induce unwanted switching in the case of (0,0) inputs is substantially higher than the typical operating voltage of 1.4 *V* and is not shown in the graph. Another possible variability in voltage sources is non-ideality of the power grid, which is modeled by a serially connected resistor (see Fig. 2). The analysis for such a source is similar to that of the bitline resistance. However, in this case the added resistance is only present on the wire connecting the gate inputs to the voltage driver, and not on the wire connected to the output. This increases the resistance value at which the gate will fail. Relevant simulation results and constraint analysis are shown in Fig. 15. Typical source resistances are a few ohms and have little to no effect on the switching time of a MAGIC NOR gate. In fact, almost no change in the switching time is observed when adding serial resistance of up to 200 Ω, at which point the gate fails to switch.

8. Corners

Process corners [43] is a popular technique in semiconductor design and manufacturing to ensure that an integrated circuit has an adequate design margin. This is achieved by determining the slow and fast corners of the technology, which are the values of process variations that lead, respectively, to the slowest and fastest switching of the circuit elements (usually CMOS transistors). A proposed design must be able to correctly function within the entire range defined by the corners. Thus, exhaustive simulations are usually conducted, using cell models operating under corner conditions to ensure that the design meets performance requirements, and that all operational condi-

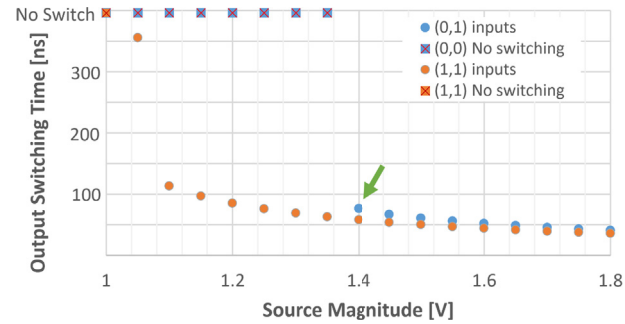

Fig. 14. Influence of operating voltage on the output switching time for different input combinations ((0,1) in blue, (1,1) in orange). The green arrow marks the baseline configuration. In the case of (0,1), a small change in the source magnitude causes the gate to go from proper functionality (dots) to failure (squares). A similar transition from functioning (dots) to failing (squares) is demonstrated for (1,1), although it requires a larger deviation of the source magnitude. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

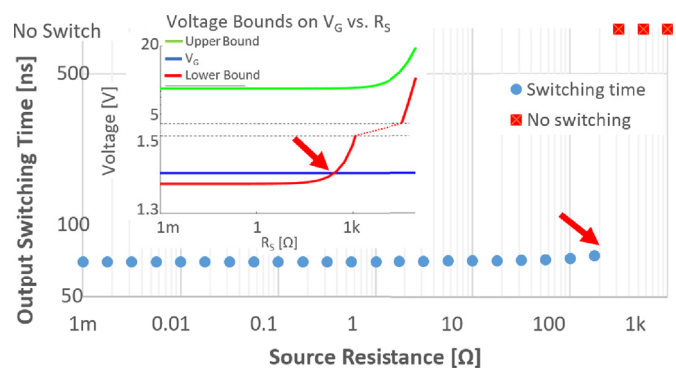

Fig. 15. Influence of supply voltage resistance on the output switching time. Red squares indicate no switching observed. Theoretic bounds on operation voltage from (4a) when considering source resistance are shown in the inset. The red arrows mark the point where the lower bound rises above the operating voltage, causing a failure in the operation of the gate. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

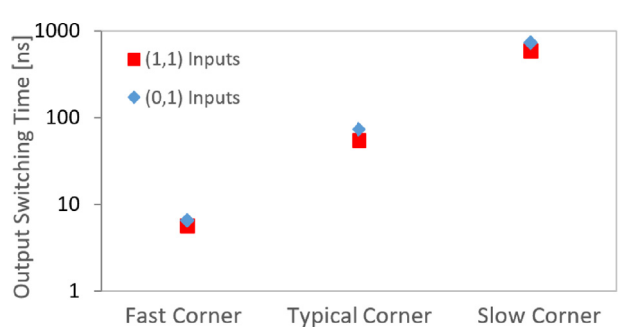

Fig. 16. Switching times for input combinations that lead to output switching using fast, typical and slow corners, as listed in Table 2.

Table 2
Example for quantitative corner analysis.

	Fast Corner	Typical Corner	Slow Corner
Wordline Resistance	0 Ω	64 Ω	128 Ω
Bitline Resistance	0 Ω	64 Ω	128 Ω
Junction Capacitance	1 fF	0.5 pF	1 pF
HRS Resistance	208 $k\Omega$	173.8 $k\Omega$	139 $k\Omega$
LRS Resistance	6.4 $k\Omega$	8 $k\Omega$	9.6 $k\Omega$
θ_S	1.2	1	0.8
θ_h	0.8	1	1.2
k_{OFF}	9.6 m/sec	8 m/sec	6.4 m/sec
Temperature	$398K(125°C)$	$298K(25°C)$	$233K(-40°C)$
Operating Voltage	1.55 V	1.5 V	1.45 V
Switching Time - (0,1)	6.53ns	73.2ns	731.4ns
Switching Time - (1,1)	5.78ns	54.8ns	589.9ns

Table 3
MAGIC NOR performance corners for discussed parameters.

Parameter		Slow Corner	Fast Corner	Comments
Added Junction Capacitance		High Capacitance	Low Capacitance	Extreme junction capacitance causes input state drift
Wordline Resistance		Output memristor on adjacent bitline to input memristor holding '1'	Output memristor on opposite edge of crossbar from input memristor holding '1'	Sensitivity depends on wire differential resistance. If accumulated to the order of R_{ON}, the gate may fail. Input drift also observed for fail conditions
Bitline Resistance		Row where logic is performed close to crossbar drivers	Row where logic is performed on opposite side of crossbar from the drivers	
Source Non-Ideality		High source resistance Low source amplitude	Low source resistance High source amplitude	Source resistance larger than R_{ON} may cause failure
Memristor Resistance	$R_{OFF,Input}$	High resistance	Low resistance	Mild dependency
	$R_{OFF,Output}$	Low resistance	High resistance	
	$R_{ON,Input}$	High resistance	Low resistance	Low variation towards the slow corner may cause gate failure
	$R_{ON,Output}$	Low resistance	High resistance	
Ion Concentration		Low ion concentration	High ion concentration	
Physical Memristor Size		Large junction height Small cross-cut area	Small junction height Large cross-cut area	
Temperature		Low temperature	High temperature	May be inverted depending on technology
Number of Inputs		Fewer inputs	More inputs	Restrictions in Ref. [17] regarding operating voltage must be fulfilled

tions (*e.g.* setup, hold conditions of flip-flops) hold. Moreover, small batches of wafers, fabricated to have corner performance, are often produced to test the design in varying environmental conditions and to ensure correct operation. We introduce the notion of 'corners' to characterize the performance impact of different parameter variations on memristive logic. An example for such an analysis is presented in Fig. 16 and Table 2. The typical corner represents a 128 × 128 array of devices, identical to the devices described in Section 3, and driven by an operating voltage of 1.5 V. The fast and slow corners are variations by ±20% in device parameters relative to the baseline, and variations of circuit parameters to the minimal and maximal possible values.

A qualitative yet more general view of MAGIC NOR corners is given in Table 3, and is valid whenever MAGIC NOR gates are used within a crossbar array topology. Each examined parameter variation direction is mapped to a slow and fast corner. If there is a risk of gate failure as a result of varying the value of a parameter, this is indicated as well. Table 3 can be used as a basis for a quantitative analysis for required device, circuit and environmental specifications.

9. Conclusions

The impact of changing environmental conditions, manufacturing parameters, and circuit design on the performance of a stateful memristive logic gate is modeled and evaluated in this paper. Evaluation is performed on an HfO_2 device, which serves as a case study for developing a methodology that can be applied to other memristive technologies. The MAGIC NOR gate is a candidate for executing logic within memory that overcomes the main bottleneck in modern computing systems – the cost of data movement. Therefore, understanding the impact of changing conditions on performance is fundamental to the efficient design of such a novel architecture. Switching time for the worst case inputs is the metric chosen for performance evaluation. The possibility of failure due to the output not switching when it should, or due to inputs changing their state, is also considered where relevant. Other metrics, such as power and area, are left for future work. Each of the evaluated parameters is expressed in the terminology of corners, and the desired values for fast and slow operation of the logic gate are presented. The formulation of operating conditions as process corners is intended to facilitate an efficient design process for future designers

of memristive logic within memory. Following the procedure demonstrated in this paper allows designers with knowledge about the process technology used for their design to ensure that the product is able to meet performance requirements across all possible operating conditions and manufacturing variations and support the integration with CMOS technology.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mejo.2019.02.013.

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