ASIC² Project:

Cache replacement policies using SRAM and MRAM

***Background**: In computing, cache replacement policies are optimizing instructions, or algorithms, that a microprogram or an HW module uses in order to manage a cache of information stored on the computer. Toggle MRAM uses a 1 transistor, 1 MTJ cell to provide a simple, high-density memory. Everspin uses a patented Toggle cell design that delivers high reliability. Data are always non-volatile for 20-years at temperature. During a read, the pass transistor is activated and data is read by comparing the resistance of the cell to a reference device. During writes, the magnetic field from Write Line 1 and Write Line 2 writes the cell at the intersection of the two lines but does not disturb other cells on either line. MRAM products employ a one transistor, one magnetic tunnel junction (MTJ) memory cell for the storage element. The MTJ is composed of a fixed magnetic layer, a thin dielectric tunnel barrier and a free magnetic layer. When a bias is applied to the MTJ, electrons that are spin polarized by the magnetic layers traverse the dielectric barrier through a process known as tunneling*

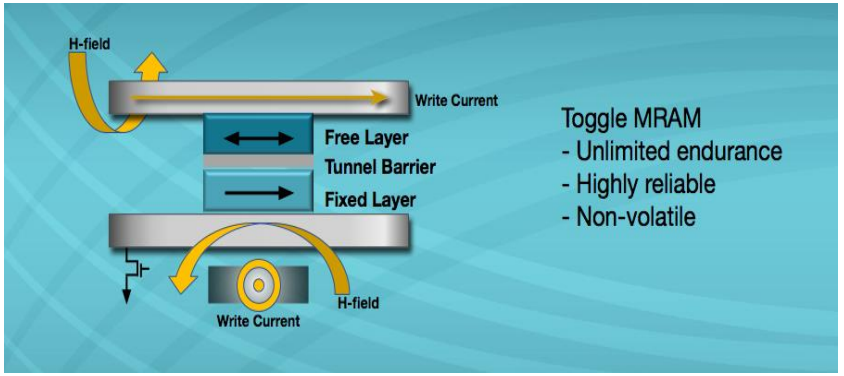
Project Description:

Study: the policies, their characteristics, and applications, the theory of Magnetic RAM and its interface,

Develop an interface on FPGA to standard SRAM 35nsec and a Toggle MRAM. Connect the circuit to the FPGA and debug the interface and compare SRAM and MRAM performances using Memory patterns.

Implement LIFO and FIFO controllers for the memories and demonstrate functionality. Implement LRU, TLRU, MRU, Pseudo-LRU, random replacement, SLRU, LFU, LFRU, LFUDA and as many policies found in the literature.

Address the nonvolatile cache issue: PROs and CONs. Propose an optimized instruction for Risc-V ISA for every implemented policy.



Prerequisites: **TBD**

Recommended: **TBD**

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