ASIC² Project:
Create and Demonstrate the Pulpenix environment on ASIC² servers using VLSI lab tools

**Background:** Pulpenix is an Enics SOC research platform primarily based on the open-source PULP platform provided by: [https://www.pulp-platform.org/](https://www.pulp-platform.org/)

More specifically, the initial Pulpenix version is based on the PULP Pulpino SOC flavor, minimal single-core SoC integrating the RISC-V RISC-V implementation.

Additionally, Pulpenix also supports a HW/SW (Hardware/Software) co-design environment, which is developed and maintained by Enics, this currently includes support of an Eclipse-based SW debug environment currently running with the platform HW simulation.

**Tasks**
- Write and compile SW.
- Show simulation.
- Make minimal HW update.
- Show simulation.
- Learn WD SwerV RISC-V implementation
- Suggest technique for Pulpino replacement by SwerV.
- Bonus: execute replacement.

**Prerequisites:** TBD

**Recommended:** TBD

**Supervisor:** Eric Herbelin,
[ericherbelin@ee.technion.ac.il](mailto:ericherbelin@ee.technion.ac.il)