A Dual-Band CMOS Low-Noise Amplifier using Memristor-Based Tunable Inductors

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***Abstract*—The growing demand for multi-band and multi-standard wireless devices requires flexible architectures that can reutilize the different blocks in the RF chains to reduce size and power consumption. The traditional multi-band radio with an RF chain per band is no longer scalable. Memristive devices have shown excellent performance as RF switches and also have a small footprint. Furthermore, as they are fabricated in the back-end of line of CMOS process, they enable tunability to integrated spiral inductors. In this paper, we present the design and simulations of a dual-band (2.4 GHz and 5 GHz) source degenerated low-noise amplifier (LNA) using memristive-via switched tunable inductors. Owing to the tunable inductor, the dual-band LNA has negligible area overhead compared to its single-band sibling. The LNA is designed using a 0.18-μm RF CMOS technology and achieves a gain of 18.8 dB and 10.3 dB at 2.4 GHz and 5 GHz, respectively, and a noise figure (NF) below 2.3 dB at both bands. In addition, we present a semi-automated design methodology for the tunable inductors.**

***Index Terms*—Memristor; memristive devices; low-noise amplifier; tunable inductor; RFIC; RF CMOS; CBRAM; resistive memory; dual-band; reconfigurable RF; NF; RF switch; phase-change RF switch;**

I. Introduction

Reconfigurable RF integrated circuits are an attractive feature to sustain the increasing number of standards and frequency bands of modern mobile devices [1]. In a reconfigurable RF architecture, the connection between different blocks, $e.g.$, mixers, analog-to-digital converters, filters, and amplifiers, can be changed (namely, inter-block reconfiguration). Conversely, each block can be reconfigured internally ($i.e.$, intra-block reconfiguration), changing the resonance frequency or some other performance parameter of the block [1]. Reconfiguration reduces the need for independent RF chains for each band, enabling block reutilization, eliminating redundant components, adding flexibility, and reducing the area overhead and the complexity of wireless front-ends. This in turn reduces the costs and the development time of a system.

Low-noise amplifiers (LNAs) have a critical role in the overall performance of receivers since they are usually the first active stage after the antenna [2]. In a reconfigurable architecture, the LNA must provide high gain, low noise figure (NF), and good input matching for multiple frequency bands. Band switching and gain switching in LNAs usually require multiple switchable amplification transistors, capacitors, and inductors to achieve the desired reconfigurability [2]. Thus, multi-band LNAs require high-performance switches since resonant narrowband circuits demand high quality factor (Q) inductors and capacitors.

Different topologies for multi-band LNAs have been proposed. In [3], a bank of cascoding transistors, each connected to a different inductor, is used to switch between bands. Another topology [4] consists of switched inductively degenerated common-source (CS) stages, each designed for a different band, using a bank of inductors. To reduce the losses and NF, emerging technologies can be used for the RF switches. For example, the use of four-terminal in-line phase-change switches (IPCS) has been proposed in [5] to improve the LNA proposed in [4]. Nevertheless, providing tunabilty in these topologies requires a significant area overhead compared to a single-band LNA. An alternative approach to support tunability is proposed in [6], where a multitapped switched inductor is used to reconfigure a multi-stage LNA with switched CS amplifiers. Despite the large area overhead of the switched CS amplifiers and the low-Q of the inductors, this approach has demonstrated that tunable inductors can provide the required reconfigurability to self-adapt to widespread frequency bands, potentially with less area overhead than a bank of inductors.

In this paper, we propose a dual-band cascode CS LNA with inductive degeneration which uses memristive tunable inductors [7] to reconfigure the amplifier between the 2.4 GHz and 5 GHz bands, which are the frequency bands allotted to the IEEE 802.11ac standard. The tunable inductor uses a conductive-bridge RAM (CBRAM) RF switch as a tunable via to connect/disconnect the top-metal layer (where the spiral loop is routed) with the cross-under (second terminal) of the inductor at the crosspoint between both layers, thus varying the inductance of the inductor between two distinctive levels. Owing to the large tunability of the memristive tunable inductors, this well-known LNA topology can be adapted to multiple frequency bands.

The use of a single CS stage and tunable inductors significantly reduces the area in multi-band RF systems, when compared to bank of inductors or switched amplifiers as proposed in [3]–[5]. As the position of the memristive switch within the spiral inductor determines the inductance value, automated determination of the switch's position is detrimental. Therefore, in this work we also propose a design method using analytical models to correctly determine its position

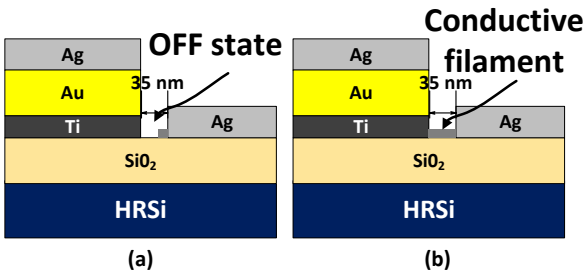


Fig. 1. Schematic structure of in-line CBRAM RF switches [14]. Two electrochemically asymmetric electrodes are separated by a 35 nm air gap. (a) HRS, the conductive filament is ruptured. (b) A conductive filament is formed between the electrodes, lowering its resistance.

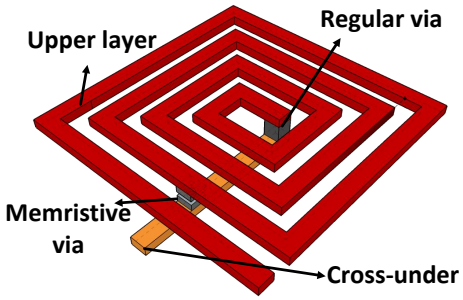


Fig. 2. 3D illustration of the memristive-via tunable inductor [7]. The square spiral loop is routed in the upper layer (red), while the cross-under is routed in a lower metal layer (gold). A memristive-via connects/disconnects these two layers.

and achieve the required inductance values. We simulate the inductors in Advanced Design Systems (ADS), a momentum 3D planar electromagnetic (EM) simulator, and extracted for full-circuit simulations in Cadence Virtuoso. Our simulation results show that the proposed LNA achieves high amplification ($\geq$10 dB) and low NF ($\leq$2.3 dB), with just $\sim$ 2% area overhead.

II. Memristive Devices in RF

A. High-Performance RF Switches

Non-volatile resistive memories (or simply memristive devices) such as resistive RAM (ReRAM), CBRAM, and phase-change memory (PCM), are passive devices whose resistance is determined by the history of a voltage or current stimulus, and retained whenever the external stimulus is no longer applied. Because of their high non-linearity, these devices can be used as switches and storage elements with a high resistive state (HRS, R_{OFF}) and a low resistive state (LRS, R_{ON}). Switching from R_{ON} to R_{OFF} is called 'reset', whereas the opposite switching is called 'set'. These devices have proven to be great candidates for memory [8], [9], logic within memory [10], neuromorphic computing [11], and recently, as high-performance RF switches [12]–[19], due to their excellent transmission properties as well as their small footprint, low power consumption and non-volatility.

These switches have exhibited promising high-frequency performance, as they achieve a state-of-the-art cutoff frequency, defined as $(2\pi R_{ON}C_{OFF})^{-1}$, where R_{ON} is the ON-state resistance and C_{OFF} is the OFF-state capacitance. The cutoff frequency is a figure-of-merit (FOM) of RF switches. These devices can be fabricated in the back-end-of-line (BEOL) of CMOS process, reducing the parasitics and area overhead associated with routing down to the substrate. Thus, memristive RF switches can provide tunability to passive devices that are fabricated in (or between) the metal layers ($e.g.$, capacitors and inductors).

CBRAM RF switches consist of two electrochemically asymmetric metal electrodes separated by a gap or a low-k insulator. A CBRAM RF switch with an air-gap of 35 nm [14] is illustrated in Fig. 1. The device is fabricated over a high-resistivity silicon substrate, in-line with a coplanar waveguide (CPW). The switching mechanism is determined by the formation/rupture of a conductive filament that changes the resistance between the electrodes. The metallic filament is formed due to electrochemical reactions, and ion migration from the active electrode, with a resistivity three times that of bulk Ag. This device achieves an R_{ON} of 2.6 Ω, an R_{OFF} of 1 TΩ, and a C_{OFF} of 1.41 fF, which means a FOM of 35 THz. The device is voltage-controlled with a set voltage of 3 V and a reset voltage of -0.4 V.

B. Tunable Inductor using Memristors

Monolithic tunable inductors find their application in resonant narrow-band circuits, $e.g.$, VCOs, LNAs, and tunable filters, basic circuits in reconfigurable multi-band architectures. Usually, integrated inductors are implemented as spiral metal structures to benefit from the mutual inductance between the turns. The performance metrics of tunable inductors are their quality factor (Q), self-resonant frequency (SRF), and tunability ratio (TR). The Q accounts for the ohmic losses, while the SRF is the maximum frequency at which the device works as an inductor. The TR is defined as $(L_{max} - L_{min})/L_{min}$ [20].

When CBRAM-based RF switches are used for tunable inductors, the memristor acts as a switchable via, which can tune the inductance of the spiral inductor with no additional routing. Fig. 2 illustrates a memristive-via tunable inductor [7]; the memristor acts as a switchable via, which can tune the inductance of the spiral inductor with no additional routing. The low ON-resistance of the memristive RF switch means that whenever the latter is in R_{ON}, the inductance will be determined by the outer loop. Conversely, when the memristive switch is in R_{OFF}, no current flows through the switch, and the inductance will thus be that of the whole spiral. Since the CBRAM RF switch is voltage-controlled, the inductor can be programmed from its two ports, without the need of additional routing.

The equivalent lumped model of the tunable inductor consists of two Π-networks as shown in Fig. 3. The inductors L_i are the self-inductance of the inner and outer loops. Capacitors C_{ox_i} model the parasitic capacitance to the substrate. Capacitors C_{S_i} are the parasitic capacitance between the spiral and the cross-under, R_i is the parasitic capacitance of the

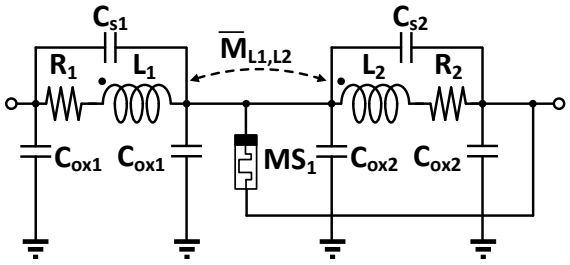


Fig. 3. Equivalent lumped model of the memristive-via. The two RLC networks represent the two sections of the spiral inductor. Inductors L_1 and L_2 are the self-inductance of the loops, while $\overline{M}_{L1,L2}$ is the mutual inductance between the two inductors. Capacitors C_{ox1} and C_{ox2} model the capacitive coupling of the loops to the substrate. Resistors R_1 and R_2 are the resistance of the loops. Capacitors C_{S1} and C_{S2} represent the coupling capacitance between the upper layer and the cross-under. MS_1 is the memristive switch.

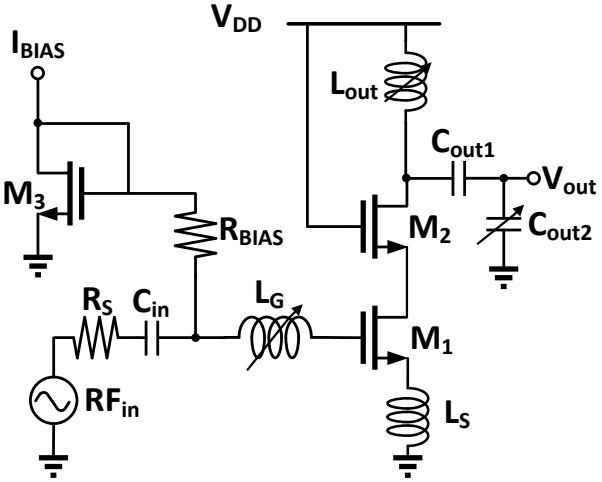


Fig. 4. Schematic of the proposed dual-band source degenerated CS LNA using memristor-based tunable inductors. In this design, L_G and L_{out} are on-chip tunable inductors, while L_S is static.

conductors, and $M_{L1,L2}$ the mutual inductance between the inner and outer loops. Finally, MS_1 is the memristive-via, *i.e.*, the CBRAM switch.

III. Tunable Common-Source LNA with Source Degeneration using Memristive Tunable Inductors

The proposed tunable LNA topology is a cascode common source (CS) with inductive degeneration LNA, as shown in Fig. 4. In this topology, the gate inductor (L_G) and the output inductor (L_{out}) are memristor-based tunable inductors. The input impedance of this circuit is

$$Z_{in} \simeq \frac{1}{j\omega C_{gs_1}} + j\omega(L_S + L_G) + \frac{g_m L_S}{C_{gs_1}} \ , \qquad (1)$$

where C_{gs_1} and g_m are the gate-source parasitic capacitance and the small-signal transconductance of transistor M_1, respectively. Note that $g_m/C_{gs} \simeq \omega_T$, the cutoff frequency of the transistor. The last term in (1) is a positive frequency-independent real impedance, which is the main advantage of the inductive degeneration. By choosing the appropriate design parameters, this term can be R_S, hence matching the source output resistance. Since the source inductor, L_S, is usually small, an inductor at the gate (L_G) is added to resonate (together with L_S) the capacitance C_{gs_1} at the desired operating frequency, eliminating the undesired reactance. To match the output, capacitor C_{out_1} and the bank of capacitors C_{out_2} resonate with inductor L_{out}.

Transistor M_2 is a cascoding transistor that reduces the Miller effect of the gate-drain capacitor (C_{gd}) of M_1, improving the stability of the LNA. Inductor L_{out} is also required to resonate the drain capacitance of M_2. Transistor M_3 forms a current-mirror with transistor M_1 to provide the operating point. Capacitor C_{in} is a DC blocking capacitor at the RF input. The bias resistance, R_{BIAS}, must be sufficiently large to reduce its noise current. Usually, resistance values over 2 $k\Omega$ are satisfactory.

Using variable inductors, the input and output of the LNA can be matched for different frequencies. Inductor L_G varies between two inductance values, to resonate C_{gs_1} at both frequency bands and thus match the input. Conversely, inductor L_{out} varies to match the output. Because of the small parasitic resistance of the inductors, the DC voltage drop in the memristive switches is smaller than the set and reset voltages.

A. Design of the Proposed Reconfigurable LNA

In this paper, we design an LNA for the popular WiFi bands, 2.4 GHz and 5 GHz. We set the same bias point for both bands, thus maintaining the same g_m and ω_T. Furthermore, L_s is static, while L_G and L_{out} are tunable. Here, the programming of the memristive switches is off-chip and a pad capacitance of 30 fF is considered. We design the CS LNA using the power-constrained optimization technique [21], [22]. This method aims to find the transistor sizing that optimizes the NF for a specific power budget. Because the NF is a function of the power consumption, which is in turn related to the transistor width, the optimal width that minimizes the NF for a specific power-constraint is

$$W_{opt_P} = \frac{1}{3\omega L C_{ox} R_s}, \qquad (2)$$

where L is the length of the transistor, and C_{ox} is the capacitance of the oxide layer at the gate. With W_{opt_P}, the minimum NF can be expressed as

$$F_{min_P} = 1 + 2.4\frac{\gamma}{\alpha}\frac{\omega}{\omega_T}, \qquad (3)$$

where γ is the excess noise coefficient, and $\alpha = g_m/g_{d0}$, where g_{d0} denotes the drain conductance. The parameters are γ =2/3 and α =1 for long-channel transistors, and γ =2 and α <1 for short-channel devices.

For this specific design we allocate a power of 10 mW to the amplifier and 1 mW to the current mirror. First, we determine the optimal transistor width using (2) for 2.4 GHz, which gives $W_{M_1} \simeq 350$ μm. For the chosen power, $g_{m_1} \simeq 70$ mS, and

$f_T = \omega_T/2\pi = 25.6$ GHz. Therefore, from (3) and with a γ of 2/3, the LNA will have an NF of 0.6 dB at 2.4 GHz. Since we use one CS CMOS transistor for both bands, the transistor width deviates by 50% from the optimal width for 5 GHz.

B. Narrowband Matching with Tunable Inductors

To match the input, we first need to determine the source degeneration inductance, L_S, that will generate an input impedance with real part of 50 Ω. As the real part of (1) is $\omega_T L_S$, $L_S = R_S/\omega_T = 310$ pH. This L_S value is updated during simulations to compensate for the parasitic C_{gd}. In first-order approximation, $Re\{Z_{in}\}$ is invariant with frequency; however, L_S is frequency-dependent and thus may differ from the value at 2.4 GHz. The gate inductor, L_G, is used to resonate the gate capacitance; thus, $L_G = 1/\omega^2 C_{gs_1} - L_S$. At 2.4 GHz, L_G is 4.8 nH and 1.8 nH at 5 GHz. The bias capacitor C_{in} must be large enough to provide DC blocking and not interfere with the matching. Hence, we choose C_{in} = 70 pF. The drain inductor, L_{out}, is used to match the output by resonating the output capacitance C_{out} and the drain capacitance of M_2. In our case, L_{out} is 6.8 nH at 2.4 GHz and 2 nH at 5 GHz. Finally, capacitor C_{out_1} is a metal-insulator-metal (MIM) capacitor of 300 fF and the bank of capacitors C_{out_2} consists of two MIM capacitors. The first of 250 fF (always connected) and the second of 650 fF switchable using a CMOS switch.

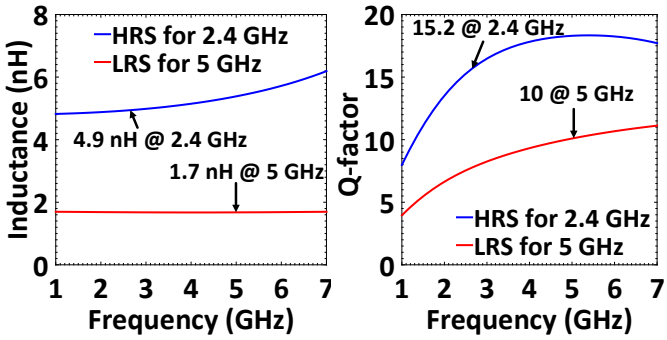
C. Semi-automated Design of the Tunable Inductors

The inductors are designed using ASITIC [23], a popular and accurate design tool for passive RFIC devices. The technology file is modified to fit our RF CMOS 1P6M 0.18 μm substrate. The first step in the design process is to find the dimensions of the entire inductor, optimizing for highest Q. Then, we find the split point by searching for the square inductor with the same outer diameter (d_{out}), width (W), and spacing (S) that leads to the required inductance at 5 GHz. We use the current-sheet expressions for square inductors [24],

$$L = \frac{1.27\mu_0 n^2 d_{avg}}{2}\left[ln\left(\frac{2.07}{\rho}\right) + 0.18\rho + 0.13\rho^2\right], \quad (4)$$

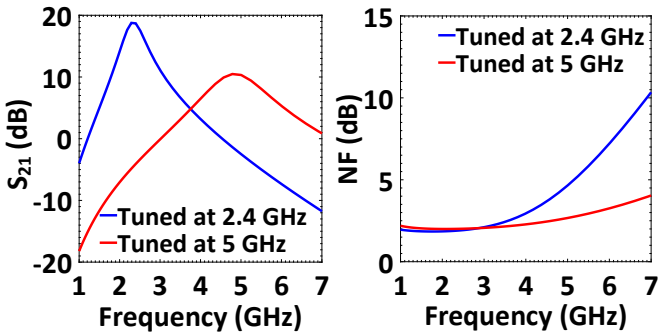
where n is the number of loops and d_{avg} is the arithmetic mean between the outer and inner diameters. Parameter ρ is the fill factor, defined as $\rho = (d_{out} - d_{in})/(d_{out} + d_{in})$.

The inductors are then implemented and simulated in ADS using the same RF CMOS substrate as in [7]. The square spirals are implemented in the top metal layer (M6). The filament of the memristor is 100 nm wide, as simulated in [7], [14], and the insulator is Ag^+-saturated $GeSe_2$, as in [12]. Inductor L_G is a 120-μm-wide square spiral, with W =4 μm, S =1.5 μm, and n =6. The changes in the inductance and Q can be observed in Fig. 5. Inductor L_{out} is 120-μm-wide square spiral, with W =4 μm, S =1 μm, and n =8.5. Finally, L_S is implemented as a 80-μm-wide square spiral with W =5 μm, S =2 μm, and n =2.5, which results in L_S =720 pH. As mentioned, L_S is increased to compensate for the parasitic C_{gd} and the pad capacitance.



(a) (b)

Fig. 5. EM simulations of L_G's (a) inductance, and (b) Q, for distinct memristive states.



(a) (b)

Fig. 6. Simulation results of the LNA for 2.4 GHz and 5 GHz. (a) S_{21}, (b) NF.

IV. Simulation Results

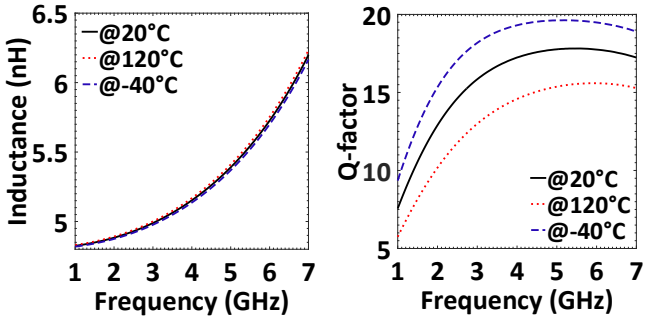
The proposed LNA circuit is simulated in Cadence Virtuoso, using a 0.18 μm technology design kit (PDK). The EM models of the inductors are loaded to the Virtuoso for full-circuit simulations. The simulated gain and NF for the two bands are shown in Fig. 6. There is a notorious gain reduction at 5 GHz, due to the large parasitic C_{gd} and the reduced Q of the inductors at this frequency. However, the obtained gain at this band is still close to the maximum available gain, and good enough when compared to other dual-band LNAs at these bands [4], [5]. Since the maximum Q is achieved at higher frequencies than these bands, gain improvements are expected. The NF is expected to increase in a fabricated circuit, but the simulations show an excellent starting point.

Thanks to the memristive-via switched tunable inductor, a single CS transistor can be used for both frequency bands, hence achieving a considerably smaller area than in previously proposed topologies. The bias point is fixed at both frequency bands to 9.4 mW, as L_S is a fixed inductor; nevertheless, this could be changed if a tunable L_S is used. Note that a change in the bias current changes the g_m, and thus the ω_T and $Re\{Z_{in}\}$. The performance of the LNA is compared to other works in Table I. The area overhead of our topology compared to a single-band inductively degenerated CS LNA is only ∼2%, and is due to the bank of capacitors.

TABLE I
PERFORMANCE COMPARISON TO OTHER DUAL-BAND LNAS

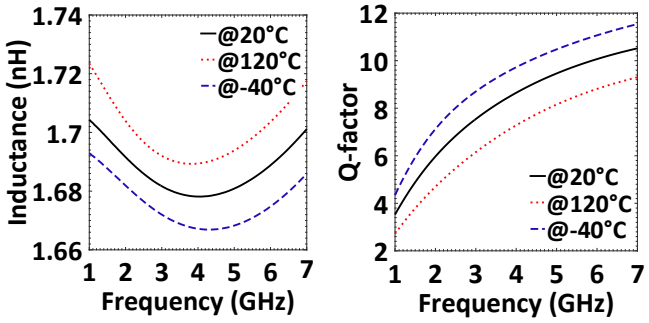
Ref.	Technology	Band	Gain (dB)	NF (dB)	IIP3 (dB)	Power (mW)	Switching Mechanism
[4]	0.18 μm CMOS	2.4 5.2	10.1 10.9	2.9 3.7	4 -5	11.7 5.7	Multiple CS stages switched by a CMOS switch + bank of capacitors at output.
[25]	0.13 μm CMOS	2.4 6	9.4 18.9	2.8 3.8	-4.3 -5.6	2.8	Switched transformer at input matching network.
[6]	0.13 μm CMOS	2.4 5.4	22.1 24.8	2.8 3.1	-18.2 -20.4	4.6	Switched CS stages (using CMOS switch) + multitapped inductor.
[5]	0.13 μm CMOS + IPCS	3 5	21.2 21.9	2.5 2.7	-12.5 -13.8	7.2 3.6	Multiple CS stages switched by a IPCS + Bank of capacitors at output.
This work*	0.18 μm CMOS + TIME	2.4 5	18.8 10.3	1.6 2.3	-15.7 2.1	10.2	Single CS stage with 2 memristor-based tunable inductor + bank of capacitors at output.

* Simulation results



(a) (b)

Fig. 7. EM simulations of L_G's variation with temperature for HRS (120°C dotted red, -40°C dashed blue, 20°C solid black). (a) Inductance, and (b) Q.



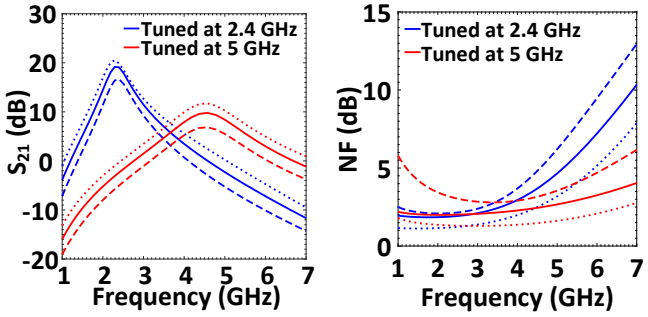
(a) (b)

Fig. 8. EM simulations of L_G's variation with temperature for LRS (120°C dotted red, -40°C dashed blue, 20°C solid black). (a) Inductance, and (b) Q.

The inductance and Q-factor variations at different temperatures are depicted in Fig. 7 and Fig. 8, for HRS and LRS, respectively. Although the changes in the inductance are almost negligible, the change in the Q-factor can affect considerably the performance of the LNA. Corner simulations (see Fig. 9) show a $\pm 10\%$ deviation in the gain and NF.

V. CONCLUSIONS

In this paper, we have presented the design and simulation of a dual-band LNA using memristor-based tunable inductors. The proposed LNA achieves high performance in



(a) (b)

Fig. 9. Simulation results of the LNA for 2.4 GHz (in blue) and 5 GHz (in red) for fast (dotted), typical (solid) and slow (dashed) conditions. (a) S_{21}, (b) NF.

both frequency bands with negligible area overhead compared to its single-frequency sibling thanks to the memristive-via switched tunable inductor, which has non-existent area overhead compared to a fixed inductor. The simulation results show that the LNA achieves low NF and competitive gain at both frequency bands. We also proposed a design methodology to use memristor-based tunable inductors in real designs by finding the optimum square spiral for maximum Q, and by determining the proper placement for the memristive switch to obtain the required inductance. Future work will focus on in-chip programming circuits for the memristive tunable inductors, design optimization for other bands, the and experimental demonstration of the proposed topology.

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