AES Add-on to RISC-V

**Background:** AES (Advanced Encryption Standard) is one of the most popular encryption algorithm today. For this purpose, we will implement the AES algorithm on a RISC-V architecture and add an AES HW to the Standard ISA.

**Project Description:**
- Hands-on RISC-V PULPINO infrastructure
- Implement and debug AES on FPGA
- Integration in RISC-V environment
- Demonstrate advantages by mean of performance

Perquisites: Computer organization and Design
Recommended: Lab1
Host Lab: High-Speed Digital Systems Laboratory
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