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Compact Modeling and Electrothermal Measurements of Indirectly Heated Phase-Change RF Switches

Nicolás Wainstein[®], *Graduate Student Member, IEEE*, Guy Ankonina, Shahar Kvatinsky[®], *Senior Member, IEEE*, and Eilam Yalon[®], *Member, IEEE*

Abstract - Four-terminal, inline, indirectly heated phasechange switches (IPCS) have emerged as great contenders for reconfigurable radio frequency (RF) integrated circuits, providing state-of-the-art cutoff frequency thanks to their built-in dc-RF decoupling. However, the switching of IPCS devices is determined by their temperature which is challenging to predict. In this article, we present a physics-based compact model of the IPCS, validated by finite-element method simulations and measurements of IPCS devices. The model accurately predicts the thermal and electrical dynamics of the device by considering the changes in heater resistance, contact resistance, and parasitic capacitance. The complete model is implemented in Verilog-A, and a downloadable version is freely available at the nanoHUB.org. We show how the compact model can be used for rapid device evaluation and optimization between RF performance and energy efficiency. Nanosecond electrical thermometry of the heater for varying pulses during IPCS device operation and RF measurements is used to experimentally validate the model.

Index Terms—Compact modeling, electrothermal, GeTe, phase-change, radio frequency (RF), RF switch, thermometry.

I. INTRODUCTION

FOUR-TERMINAL, inline, indirectly heated phase-change radio frequency (RF) switches (IPCS) have recently emerged as great contenders for 5G, mmWave, and reconfigurable RF circuits [1]–[9], owing to their excellent transmission properties, nonvolatility, small footprint, high switching endurance, and CMOS compatibility. These devices exhibit order-of-magnitude better cutoff frequency ($f_{\rm CO} = (2\pi\,R_{\rm ON}C_{\rm OFF})^{-1}$, where $R_{\rm ON}$ is the ON-resistance, and $C_{\rm OFF}$ is the OFF-capacitance) over standard semiconductor technologies [10]–[13].

The IPCS consists of a phase-change material (PCM) connected inline by two RF ports. The PCM is thermally activated

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The authors are with the Andrew and Erna Viterbi Faculty of Electrical Engineering, Technion – Israel Institute of Technology, Haifa 32000, Israel (e-mail: nicolasw@campus.technion.ac.il).

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from beneath by an embedded heater, which is isolated from the PCM by a dielectric material. The thermal actuation of a PCM poses a critical challenge to device and circuit designers because the device temperature must be known to determine the switching characteristics (i.e., switching voltage and power). The switching voltage and power are tightly related to the lateral dimensions of the IPCS even if the thickness of the layers is kept constant. The design criteria of IPCS are explored in [6], showing the dependence of the RF and thermal performance on the device structure.

In [14] and [15], finite-element method (FEM) simulations of the melt/quench process in IPCS were studied, and the energy efficiency was explored. The electrical thermometry of bare microheaters only (e.g., not complete devices) were reported in [15] to validate the FEM model. In [16], an electrothermal model of directly IPCS [17] is reported. This model uses the frequency-domain solution of the heat transfer function to predict the maximum power handling of these switches. This model was adapted in [18] and [19] to predict the maximum power handling of indirectly heated devices, as the RF signal can also heat directly (and switch) the PCM layer.

Currently, a computer-efficient compact model that can rapidly predict the dynamic behavior of the IPCS in a circuit environment is still lacking. Such a model is critical for fast device design and optimization and to design its peripheral circuitry. In this article, we present a compact model of the IPCS device. The thermal dynamics are modeled using a thermal-equivalent RC model, based on the physical dimensions and thermal properties of the device. The temperature feeds a behavioral model that determines if a phase transition occurs. The electrothermal model is validated using FEM simulations and experimental electrical thermometry of complete GeTe IPCS devices with different physical dimensions. Furthermore, the compact model can predict the RF performance of the device. Here, the RF behavior of the IPCS is modeled similar to the lumped models presented in [5], [6], and [19]. The advantage of the model is that the lumped elements are analytically determined by the dimensions of the device and not by fitting as in the previous works. The lumped RF model is validated with RF measurements.

The compact model is implemented in Verilog-A (SPICE-compatible). Thus, it enables rapid device optimization, and

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Fig. 1. **Fabricated GeTe IPCS.** (a) Schematic cross section. (b) False-colored SEM image. A PCM is connected in line by two RF electrodes of width $W_{\rm RF}$, separated by a small gap of length $L_{\rm RF}$. The PCM layer is thermally activated from beneath by a heater of width W_H and length L_H .

the design and simulation of large-scale circuits and systems composed of IPCS with varying substrates, dielectrics, and PCM materials. The model is freely available online at the nanoHUB.org [20]. The threshold voltages and the temperature of the heater are predicted within 92% accuracy by the model. We show experimentally that the devices can be programed with lower voltage and power than the previous works [1]–[3], [5]–[7], [9], [21] by using wider pulses, as the model predicts. Furthermore, we present the electrical thermometry of operating IPCS devices, whereas the previous work [15] reported only thermometry of bare heaters.

II. DEVICE DESIGN AND FABRICATION

The cross section and scanning electron microscope (SEM) view of the IPCS are shown in Fig. 1. A 100-nm GeTe layer is connected in line by two RF electrodes of width W_{RF} , separated by a small gap of length L_{RF} . The GeTe layer is thermally activated from beneath by a heater of width W_H and length L_H . The actuation path and the RF path are electrically isolated, allowing for dc-RF decoupling. Increasing the thickness of this layer is beneficial to the RF performance but at the expense of power and energy efficiency since more heat is required to achieve switching temperature. The RF performance of the IPCS is mainly determined by L_{RF} , W_{RF} , and W_H [5], [6]. A smaller L_{RF} or wider W_{RF} reduces R_{ON} . However, widening W_{RF} will result in a larger C_{OFF} , which is mainly determined by the parallel-plate capacitance between the RF electrodes and the coupling capacitance between the RF electrodes and the heater.

The physical limit of $R_{\rm ON}$ as $L_{\rm RF}$ is scaled down and is determined by the contact resistance between the PCM and the metal electrodes. $R_{\rm ON}$ can also be reduced by increasing the thickness of the PCM layer, but this will result in larger thermal capacitance of the PCM which will degrade switching speed, power, and energy. The heater dimensions determine its electrical resistance, crucial to achieve sufficient power to switch the device. Device segmentation, as in [6], is a possible solution to reduce the programming voltages with almost negligible RF performance degradation.

The IPCS devices are fabricated on high-resistivity Si wafers. First, a 100-nm SiO₂ layer is thermally grown, followed by W dc magnetron sputtering (100 nm), and pattering by reactive-ion etch (RIE). A Si₃N₄ insulating layer (50 nm) is then deposited using plasma-enhanced CVD. The 100-nm GeTe layer is then dc sputtered and heated *in situ* up

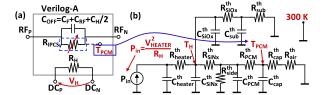


Fig. 2. Compact electrothermal model of the IPCS. (a) Macro model of the IPCS. RF $_P$ and RF $_N$ are the RF ports (where the resistance change occurs). dc $_P$ and dc $_N$ are the actuating terminals (heater). T_{PCM} is estimated to determine whether the R_{IPCS} will change or not. (b) Lumped RC equivalent model of the thermal dynamics in the IPCS.

to 200 °C, followed by patterning and etching with RIE. Premetallization surface treatment of 3-min descum and 5-min deionized water (DI) is carried out based on [22], and Ti(10 nm)/Au(150 nm) contacts are e-beam evaporated by lift-off. Finally, the GeTe is capped with 50-nm RF sputtered SiO₂, patterned by RIE, and the vias to heater pads are opened through the Si₃N₄ and metallized by Ti (10 nm)/Au (150 nm).

III. COMPACT MODEL OF IPCS

The proposed model is fully implemented in Verilog-A and consists of four electrical ports: two RF ports (RF $_P$ and RF $_N$) and two actuation ports (dc $_P$ and dc $_N$) as shown in Fig. 2(a). The change in the resistance of the IPCS ($R_{\rm IPCS}$) and the parasitic $C_{\rm OFF}$ are probed between the RF ports, whereas the programming pulse is applied to the actuation ports. The input resistance of the latter ports is the resistance of the heater (R_H). The model is subdivided in: 1) a behavioral model that determines the variation in $R_{\rm IPCS}$ and R_H according to the temperature of the PCM ($T_{\rm PCM}$) and the heater (T_H) and 2) an equivalent lumped thermal-impedance RC model [23], [24] that predicts T_H and $T_{\rm PCM}$ as shown in Fig. 2(b).

The thermal conduction is ruled by the Fourier's law of conduction, $\dot{Q} = -k\nabla T$, where \dot{Q} is the heat flux density, k_{th} is the thermal conductivity of a material, and ∇T is the temperature gradient. Assuming 1-D heat flow, the thermal resistance for a material with thickness x and area A can be defined as $R_{\rm th} = x/(k_{\rm th}A)$. The temperature variation is also governed by the change in the internal energy due to the heat flow (Q) through the device, which is determined by the specific heat capacitance (c_v) of each layer. Therefore, the thermal capacitance will be $C_{th} = c_v V$, where V is volume. The two most widely used thermal models are the Cauer and Foster models. The former is correlated with the physical structure of the device, whereas the latter is a mathematical fitting model of the measured results. In this work, we use the Cauer model since knowing the temperature of the PCM is critical to determine whether the phase has changed. In this model, we assume 1-D (vertical) heat flow, except for (lateral) heat spreading in dielectric 2 [Fig. 1(a)] represented by R_{side} . The latter assumption holds when the heater dimensions are large compared with the thermal healing length (~ 100 nm in typical IPCS devices) [15].

The design parameters of the model are W_H , W_{RF} , L_{RF} , and the thicknesses of the different layers. For simplicity, L_H is chosen to be equal to W_{RF} , and the OFF-resistance is provided

as fitting parameter to the model. With these parameters, the model determines the thermal resistances and capacitance, ON-resistance ($R_{\rm ON}$), $C_{\rm OFF}$, and the electrical resistance of the heater at room temperature ($R_{\rm HgT}$). $R_{\rm ON}$ is determined as

$$R_{\rm ON} = 2R_{C_{\rm PCM}}/W_{\rm RF} + R_{\rm sh_{PCM}}L_{\rm RF}/W_{\rm RF} \tag{1}$$

where $R_{C_{\text{PCM}}}$ is the contact resistance per unit length, and $R_{\text{sh}_{\text{PCM}}}$ is the sheet resistance of crystalline PCM. The parasitic capacitance depends on the connection of the heater while the RF signal is applied. If the pads are floating, $C_{\text{OFF}} = C_F + C_{\text{RF}} + C_H/2$ [6], where C_F is the fringe capacitance between the heater pads and the RF path, $C_{\text{RF}} = \varepsilon_0 \ k W_{\text{RF}} t_c/L_{\text{RF}}$ is the parallel plate capacitance between the RF contacts, and C_H is the coupling capacitance between the RF contacts and the heater, modeled as the fringe capacitance of a wire [25]. The resistance of the heater is

$$R_H = 2R_{C_H}/W_H + R_{\rm sh_H}L_H/W_H \tag{2}$$

where R_{C_H} is the contact resistance per unit length, and $R_{\rm sh_H}$ is sheet resistance of the heater. The electrical resistance of the heater increases with temperature as

$$\Delta R_H = R_{H_{\rm RT}} \cdot {\rm TCR} \cdot \Delta T_H \tag{3}$$

where TCR is the temperature coefficient of resistance, which is experimentally characterized in the W heaters, $TCR_W = 1.3 \cdot 10^{-3} \text{ K}^{-1}$.

Parameters $R_{C_{PCM}}$, $R_{Sh_{PCM}}$, R_{C_H} , and R_{Sh_H} are obtained from the measurements of transfer-length method (TLM) structures that are fabricated with the IPCS devices, and the extracted values are $10 \Omega \cdot \mu m$, $33 \Omega/sq$, $15 \Omega \cdot \mu m$, and $3.6 \Omega/sq$, respectively. The C_F is extracted from RF measurements as in [6] and equals 3.6 fF. The k_{th} of W and GeTe are estimated from the measured electrical conductivity using Wiedemann-Franz law, leading to $k_{\text{th}_W} = 20.3 \text{ WK}^{-1}\text{m}^{-1}$ and $k_{\text{th}_{\text{GeTe}}} = 2.2 \text{ WK}^{-1} \text{m}^{-1}$, respectively. The remaining parameters are estimated using thermal properties taken from the literature [26]–[31]: $k_{\text{th}_{\text{Si}}} = 4 \cdot 10^4 / \text{T WK}^{-1} \text{m}^{-1}$ and $k_{\text{th}_{\text{SiOx}}} = \ln(T^{0.52}) - 1.6 \text{ WK}^{-1} \text{m}^{-1}$, where T is in K. For Si₃N₄ $k_{\text{th}_{\text{SiNx}}} =$ 3 WK⁻¹m⁻¹. The thermal boundary resistance (TBR) of the SiO₂–W interface is estimated to be equivalent to the thermal resistance of 20 nm SiO₂, and TBR of the Si-SiO₂ interface is negligible [15]. The side heat spreading is modeled by $R_{\text{side}}^{\text{th}} = 10(R_{\text{sub}} + R_{\text{SiOx}})/(1 + 2L_{\text{heal}}/W_H)$, where $R_{\text{sub}}^{\text{th}}$ and $R_{\rm SiOx}^{\rm th}$ are the thermal resistances of the substrate and SiO₂, respectively, whereas L_{heal} is the thermal healing length of the heater. The electrical and thermal parameters used in the model are shown in Table I. The expressions that determine the circuit elements for the lumped electrothermal model and the RF model are shown in Table II.

When a pulse is applied to the actuation ports, a polynomial voltage-controlled current source converts the applied voltage into the input power for the thermal-impedance model. To amorphize (reset) the PCM, $T_{\rm PCM}$ must rise above its melting point ($T_{\rm M} \simeq 720~{\rm ^{\circ}C}$) and quickly quench to low temperature (i.e., below the crystallization temperature, $T_{\rm crys}$) so that the PCM does not recrystallize. For crystallization (set), $T_{\rm PCM}$ must rise above $T_{\rm crys}$ for sufficient time (i.e., crystallization

TABLE I
PARAMETERS OF COMPACT MODEL

Thermal Parameters					
Parameter	Value	Parameter	Value		
$k_{th_{GeTe}}$	2.2 W/(K·m)	$c_{v_{GeTe}}$	3.07· 10 ⁶ J/(Km ³)		
k_{th_W}	20.3 W/(K·m)	c_{v_W}	2.58· 10 ⁶ J/(Km ³)		
$k_{th_{SiOx}}$	$ln(T^{0.52})-1.6 \text{ W/(K·m)}$	$c_{v_{SiOx}}$	$2.27 \cdot 10^6 \text{ J/(Km}^3)$		
$k_{th_{Si}}$	$4 \cdot 10^4 / T \text{ W/(K·m)}$	$c_{v_{Si}}$	1.66· 10 ⁶ J/(Km ³)		
$k_{th_{SiNx}}$	3 W/(K·m)	c_{v_W}	2.28· 10 ⁶ J/(Km ³)		
TCR	$1.3 \cdot 10^{-3} \text{ K}^{-1}$	L_{heal}	100 nm		
Electrical Parameters					
Parameter	Value	Parameter	Value		
$R_{C_{PCM}}$	$10 \ \Omega \cdot \mu m$	$R_{sh_{PCM}}$	33 Ω/sq		
R_{C_H}	15 $\Omega \cdot \mu m$	R_{sh_H}	$3.6~\Omega/sq$		

TABLE II
CIRCUIT ELEMENTS OF COMPACT MODEL

Thermal RC Model					
Parameter	Expression	Parameter	Expression		
A	$W_H L_H$	R_{air}	10·10 ⁶ KW ^{−1}		
R_{sub}^{th}	$1/(2k_{th_{Si}}A)$	C^{th}_{sub}	$c_{v_{Si}}t_{Si}A$		
R_{SiOx}^{th}	$t_{d1}/(k_{th_{SiOx}}A)$	C_{SiOx}^{th}	$c_{v_{SiOx}}t_{d1}A$		
R_{heater}^{th}	$t_h/(k_{th_W}A)$	C_{heater}^{th}	$c_{v_W} t_H A$		
R_{TB}^{th}	$t_{d2}/(k_{th_{SiNx}}A)$	C_{TB}^{th}	$c_{v_{SiNx}}^{th}t_{d2}A$		
R_{GeTe}^{th}	$t_{PCM}/(k_{th_{GeTe}}A)$	C^{th}_{GeTe}	$c_{v_{GeTe}}t_{PCM}A$		
$R_{capping}^{th}$	$t_{cap}/(k_{th_{SiOx}}A)$	$C_{capping}^{th}$	$c_{v_{SiOx}}t_{cap}A$		
TBR	$20 \ nm/(k_{th_{SiOx}}A)$	R_{side}^{th}	$\frac{10(R_{sub}^{th} + R_{SiOx}^{th})}{1 + 2L_{heal}/W_H}$		

Electrical & RF Model			
Parameter	Expression		
R_{ON}	$2R_{C_{PCM}}/W_{RF} + R_{sh_{PCM}}L_{RF}/W_{RF}$		
R_H	$2R_{C_H}/W_H + R_{sh_H}L_H/W_H$		
C_{RF}	$arepsilon_0 arepsilon_{ox} W_{RF} t_{cont} / L_{RF}$		
C_H	$\varepsilon_{SiNx}L_H\left[0.77 + 1.06\left(\left(\frac{W_H}{t_{d2}}\right)^{0.25} + \left(\frac{t_H}{t_{d2}}\right)^{0.5}\right)\right]$		
C_F	6~fF		
C_{OFF}	$C_F + C_H/2 + C_{RF}$		

time, $t_{\rm crys} \geq 1~\mu {\rm s}$). From the electrothermal measurements, we estimate $T_{\rm crys}$ at $t_{\rm crys} = 1~\mu {\rm s}$ to be $\sim 450~{\rm c}$, confirmed by recent thermoreflectance measurements [32]. Thus, the behavioral model works as follows. If $T_{\rm PCM} > T_M$ and the quenching time is shorter than 250 ns, the $R_{\rm IPCS}$ will reset. Whenever $T_{\rm cryst} < T_{\rm PCM} < T_M$, the set process is triggered. If $T_{\rm PCM}$ stays between those boundaries for at least 1 $\mu {\rm s}$, then $R_{\rm ON}$ is achieved. Otherwise, $R_{\rm IPCS}$ remains unchanged.

Note that the physical dimensions of the devices (W_{RF} , L_{RF} , W_H), the thickness of the layers, and the thermal parameters can be changed to model different device geometries or materials and to perform variability analysis. For instance, if the material or deposition conditions of the heater are changed, its resistance (R_{C_H} , $R_{\rm sh_H}$), and TCR will change [5], [6], affecting the overall electrothermal performance of the device (captured by the model). The compact model presents some limitations, namely, it does not include: 1) the temperature dependence of $k_{\rm th}$ for some layers and the TCR of the heater; 2) temperature rise due to direct heating through the RF electrodes; and

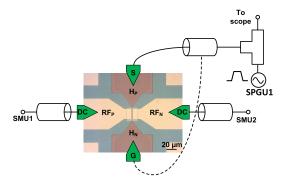


Fig. 3. **Electro-thermal measurements setup.** The heater voltage is measured using SG probes, connected in parallel to the scope in high *Z*. The RF path is probed using two SMUs of the B1500A.

3) crystallization kinetics (currently the model assumes that the PCM will crystallize if $T_{PCM} > T_{cryst}$ for 1 μ s).

IV. MEASUREMENT SETUP

Transient electrothermal measurements are performed using a Keysight B1500A semiconductor parameter analyzer (SPA) with high-voltage semiconductor pulse generator unit (HV-SPGU). A Keysight Infiium DSOS804A scope in high Z, connected in parallel to the signal-ground (SG) RF probe used to program the device, measures V_H (Fig. 3). The reset and set pulses are 800 ns and 1 μ s wide, respectively, with 50 ns rise time and 20 ns fall time. Relatively long reset pulses are chosen to have a better understanding on the heating time of the heater. The resistance of the IPCS is then measured in dc, using a four-probe setup.

The heater voltage is $V_H = 2V_{\rm app}R_H/(R_S + R_H)$, where $V_{\rm app}$ is the voltage applied by the SPGU to a 50 Ω load, and R_S is the source resistance of the HV-SPGU set to 50 Ω . The resistance of the IPCS is probed using standard dc probes connected to the semiconductor measurement unit (SMU) of the B1500A after the programming pulse is applied.

The TCR was measured using a Linkam thermal stage measuring the TLM heater structures at varying temperature, from 25 °C to 300 °C. RF measurements were performed using a Keysight Streamline USB vector network analyzer with ground-signal-ground (GSG) Cascade air co-planar (ACP) probes. The RF measurements were calibrated using the short-open-load-thru (SOLT) standard. No deembedding was performed.

V. RESULTS AND MODEL VALIDATION

The sheet resistance and contact resistance of the GeTe layer are extracted using TLM structures with 20- μ m width and length varying from 2 to 20 μ m [Fig. 4(a)]. The TCR of the W-heaters was extracted from TLM structures with $W_H=2~\mu$ m. The resistance variation of the heater with temperature is shown in Fig. 4(b) for a 40 μ m-long heater measured from 25 °C to 300 °C.

As T_H rises, R_H increases, changing V_H until a steady-state temperature is reached (few hundred ns). The change in heater resistance (ΔR_H) is probed by measuring $\Delta V_H = V_{H_{\text{max}}} - V_{H_{\text{RT}}}$, where $V_{H_{\text{max}}}$ is the maximum voltage drop at the heater when the programming pulse is applied and $V_{H_{\text{RT}}}$.

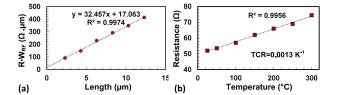


Fig. 4. **DC characterization.** (a) TLM of the GeTe PCM layer. (b) Measured TCR W-heater.

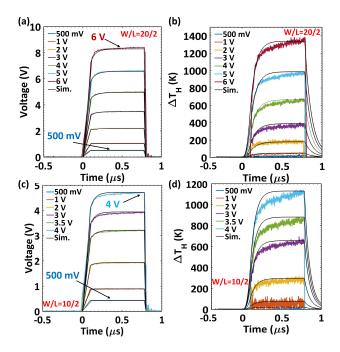


Fig. 5. Measured versus simulated electrical thermometry. Measured (colored) and simulated (black). (a) Heater voltage V_H and (b) temperature rise ΔT_H for the reset of a 2- μ m-wide and 20- μ m-long heater. (c) V_H and (d) ΔT_H for reset of a 2- μ m-wide and 10- μ m-long heater.

With the ΔV_H , ΔR_H is calculated and converted to ΔT using the TCR value. Fig. 5(a) and (b) shows the simulated versus measured V_H and ΔT_H for a $L_{\rm RF}=W_H=2~\mu{\rm m}$ and $W_{\rm RF}=20~\mu{\rm m}$ device, whereas Fig. 5(c) and (d) shows the results, respectively, for $W_{\rm RF}=10~\mu{\rm m}$ device. Note that in Fig. 5(b) and (d), the quenching time is not captured since the measured V_H signal is lost after the 20-ns fall time of the applied voltage pulse.

Fig. 6(a) and (b) shows the simulated ΔT_H and ΔT_{PCM} for a 4.5- V pulse and the temperature distribution from FEM simulations, respectively. It can be observed that the ΔT_{PCM} is correctly predicted. Fig. 6(c) shows the compact-model-predicted ΔT_{PCM} and FEM simulations for different amplitudes and varying pulsewidth. A $\Delta T \sim 150$ K is observed between 100- and 200-ns-wide pulses, confirming the advantage of using wider pulses to reduce the switching power. The maximum deviation of the simulated V_H from the experimental measurements is less than 1.5%. The error in predicting the ΔT of the heater is less than 5% for T < 1000 K and smaller than 10% for T > 1000 K. This deviation is related to changes in k_{th} of the different layers and variations of the TCR over a large range of temperatures. The switching behavior for

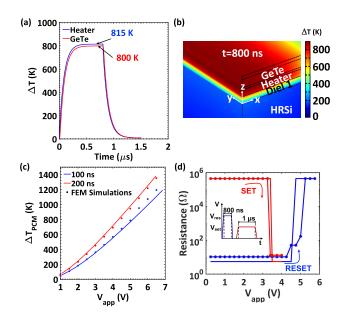


Fig. 6. Measured and simulated electrothermal behavior and switching characteristics. (a) ΔT of heater and PCM for a 4.5 V pulse precited by the compact model. (b) Temperature map of the device simulated by FEM for the same pulse as in (a). (c) ΔT on the top of PCM versus applied voltage for varying pulsewidth (lines represent compact modeling, and dots correspond to FEM simulations). (d) Measured versus simulated switching characteristics. $V_{\rm app}$ is the applied voltage from the HV-SPGU for a $50~\Omega$ load. Inset: programming pulses.

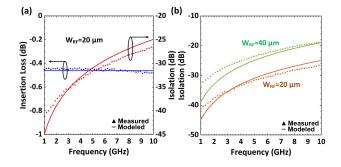


Fig. 7. Measured and simulated RF performance and power efficiency. (a) Measured (triangle markers) versus modeled (solid line) RF transmission for $W_H = L_{\rm RF} = 2~\mu{\rm m}$ and $W_{\rm RF} = 20~\mu{\rm m}$. (b) Measured (triangle markers) versus modeled (solid line) isolation of $W_{\rm RF} = 20~\mu{\rm m}$ and $W_{\rm RF} = 40~\mu{\rm m}$ switches.

reset and set is shown in Fig. 6(d). The measured minimum power for amorphization (MPA) and minimum power for crystallization (MPC) [6] are 0.51 and 0.23 W, respectively, for 20- μ m-wide devices. The corresponding threshold voltages ($V_{\rm th}$) are 5.2 and 3.4 V. The simulated MPA and MPC are, respectively, 0.46 and 0.25 W, corresponding to 4.8 and 3.5 V.

The measured and modeled RF performance is shown in Fig. 7(a) for an IPCS with $L_{\rm RF}=W_H=2~\mu{\rm m}$ and $W_{\rm RF}=20~\mu{\rm m}$. The device presents an insertion loss <0.48 dB and an isolation >26 dB up to 10 GHz, leading to an $f_{\rm CO}$ of 3.5 THz. Note that the modeled insertion loss in Fig. 7(a) includes the losses of the signal trace (estimated 0.08 dB). The modeled and measured isolation for 20- $\mu{\rm m}$ -wide and 40- $\mu{\rm m}$ -wide IPCS is shown in Fig. 7(b), and the estimated vs. measured RF parameters are shown in Table III. The compact model can be used for the rapid evaluation of IPCS device design. For

TABLE III
SIMULATED VERSUS MEASURED RF PERFORMANCE

W _{RF}	Parameter	Simulated	Measured
20 μm	$R_{ON} (\Omega)$	4.3	4.8^{-1}
	$C_{OFF} fF$	8.7	7.5
	f_{CO}	3.5	3.53
40 μm	R_{ON}	2.15	5 ²
	C_{OFF}	19	18.8
	f_{CO}	3.9	1.7

¹ As-deposited.

² Degraded R_{ON} owing to voids.

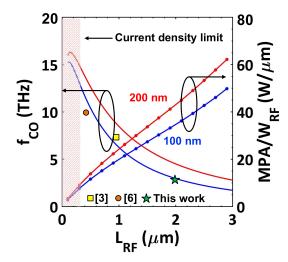


Fig. 8. RF performance versus power efficiency $f_{\rm CO}$ for a 20- μ m-wide switch and MPA per switch width for $L_{\rm RF}=W_H$ varying from 100 nm to 3 μ m, for $t_{\rm PCM}=100$ nm (blue) and 200 nm (red).

example, the $f_{\rm CO}$ for a 20- μ m-wide switch and the MPA per switch width is shown in Fig. 8 when $L_{\rm RF}=W_H$, with $L_{\rm RF}$ varying from 100 nm to 3 μ m. Due to the wider reset pulses, the $V_{\rm th}$ s in the devices are reduced compared to [1]–[3], [6], [7], [9]. Experiments on 20- μ m-wide devices with 300-ns-wide reset pulses show that the MPA may increase up to 0.8 W. The obtained $R_{\rm ON}$ is slightly higher than the one obtained with TLM structures due to the steep topographic change caused by the heater, which forms voids in the PCM layer as described in [5] and [33]. These voids also cause reliability issues, such as increasing the $R_{\rm ON}$ after a number of cycles. This can be avoided in planarized devices [34].

VI. CONCLUSION

In this article, we presented a physics-based compact model for IPCS devices. The model is fully implemented in VerilogA, allowing for fast device and circuit design and optimization. We compared the model to experimental electrical thermometry, RF measurements, and FEM simulations, showing its accuracy in simulating the electrothermal dynamics of the switch. The compact model can rapidly predict the threshold voltage, device temperature, relevant power figures of merit (MPA, MPC), and f_{CO} with 92% accuracy.

We show that IPCS devices can be programed with lower actuation voltages than the previous reports by using wider

pulses, thanks to the smaller ΔT between the PCM and the heater. Overall, we expect that the work will help make IPCS technology more accessible to device, circuit, and system designers. In the future work, we will extend the model to account for the crystallization kinetics and possible direct heating through the RF electrodes. Furthermore, we will extend the valid frequency range by including second order parasitic effects such as coupling capacitance to the substrate.

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