SW MEMORY EMULATOR PLATFORM: NEW PROJECT

Eric Herbelin <ericherbelin@ee.technion.ac.il>

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To: Inna Rivkin <inna@ee.technion.ac.il>
Cc: Mony Orbach <mony@ee.technion.ac.il>; Tom Dovlekaev <tomdovlekaev@campus.technion.ac.il>; Ephraim Zamir <ephraim@campus.technion.ac.il>

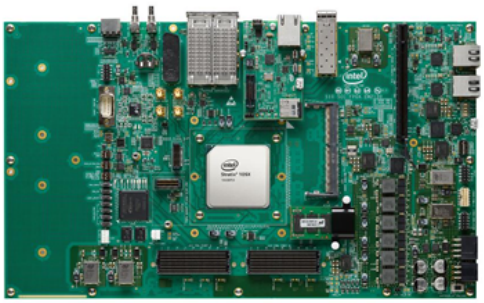
הי

בעקבות שיחתנו , בבקשה להכניס את הפרויקט הבא למערכת:

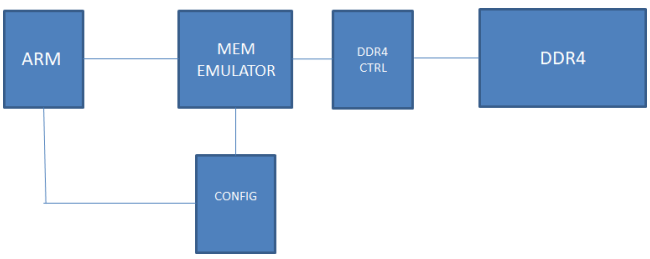
SMEP: In order to emulate new and not yet available HW memory technologies, we propose to build a configurable FPGA platform. Since the project is a cooperation with the GenPro (generic open source processor) consortium of the Innovation Authority, the implementation will use RISC-V devices of WDC consortium member.

Project:

- Learn:
  - Emerging memory technologies and their characteristics
  - RISC-V in general and SwerV-EH1 and Swerv-EL2 in details
- Get hands-on:
  - Stratix 10 Intel FPGA board: read-write to external DDR4 using both terminal and embedded ARM



  - Previous implementations of ***SweRV*** -EH1 and ***SweRV*** -EL2 on ASIC^2 Lab servers



- Implement MEM Emulator using HW Verilog Pipeline. Proceed to simulation and compare results to Expected theoretical performance by means of system clocks.
- Implement MEM Emulator using ***SweRV*** . Compare implementations.

- RRAM case: Proceed to 32b MAGIC operation. Analyze results, Propose ISA optimization.
- OPT: Demo during GenPro technology meeting.

מנחה: אריק הרבלין
סטודנתים: CC

Best Regards
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Eric Herbelin
Tel: +972778871317
Cel: +972544946383
ASIC^2 Technion Research Group
http://asic2.group/