Implementation of WDC RISC-V family processors on FPGA, benchmarking and comparison

RISC-V (pronounced "risk-five") is an open-source hardware instruction set architecture (ISA) based on established reduced instruction set computer (RISC) principles.The project began in 2010 at the University of California, Berkeley, but many contributors are volunteers not affiliated with the university. RISC-V is a new architecture that is available under open, free and non-restrictive licences. It has widespread industry support from chip and device makers, and is designed to be freely extensible and customisable to fit many applications. RISC-V is a classic RISC architecture rebuilt for modern times. At its heart is an array of 32 registers containing the processor's running state, the data being immediately operated on, and housekeeping information. RISC-V comes in 32-bit and 64-bit variants, with register size changing to match.

Western Digital **SweRVCore EH1** is a 32-bit, 2-way superscalar, 9 stage RISC-V pipeline core. **SweRVCore EH2** was built off of the EH1, but adds dual threaded capability for additional performance. **SweRVCore EL2** is a smaller core with moderate performance. It was designed to replace state machines and other logic functions in SoCs.

Project Requirements :

- Using ASIC2 servers infrastructure learn and run both EL2 and EH1
- Using HSDSL lab FPGA implement both processors on FPGA, run Hello World
- Learn relevant Benchmarks, Check the enhanced performance of the double issue capability
- Demonstrate, report and advise. Share the results on GitHub

This project is proposed in co-operation with the ASIC^2 (Architectures, Systems, Intelligent Computing Integrated Circuits lab).
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