

Indirectly Heated Switch as a Platform for Nanosecond Probing of Phase Transition Properties in Chalcogenides

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Abstract—Although phase-change materials (PCMs) have been studied for more than 50 years, temperature-dependent characterization of the phase transition dynamics remains challenging due to the lack of nanosecond-nanoscale thermometry. In this article, we utilize the four-terminal, indirectly heated phase-change switch (IPCS), which was originally designed for nonvolatile radio frequency (RF) applications, as an ultrafast electrothermal platform to study PCM. We propose a novel experimental setup that allows nanosecond probing of the transient resistance of the PCM, beyond the melting temperature (> 1100 K), due to the built-in electrical isolation between the PCM path and the thermal actuation path of the IPCS. The embedded metallic heater can induce reversible phase transitions between the crystalline and amorphous phases of the PCM. Our platform enables simultaneous measurements of the dynamics of PCM resistance (as a probe for the phase of the material) and heater temperature, during the application of heating pulses. Furthermore, we map the surface temperature of the IPCS at steady state by scanning thermal microscopy (SThM) and show the effect of cooling by electrodes in devices with overlap between the heater and PCM contacts. Our method can be used to study chalcogenides and other amorphous semiconductors for reconfigurable electronics and neuromorphic hardware.

Index Terms—Chalcogenides, crystallization, electrothermal, GeTe, phase-change memory, thermometry.

I. INTRODUCTION

CHALCOGENIDE phase-change materials (PCM) are technologically attractive materials for nonvolatile memory [1], neuromorphic computing [2], [3], optoelectronics [4],

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and, recently, radio frequency (RF) [5]–[9] applications. These materials present a large resistance ratio ($> 10^3$) between the crystalline (low resistivity) and amorphous phase (high resistivity). The phase transition is thermally activated, and its kinetics can span orders of magnitude in time, from several seconds down to subnanosecond timescale. Thus, proper characterization of the thermal behavior is required to understand the fundamental material properties of PCMs, particularly the physics of melt-quench processes in nanoscale devices, interface versus bulk, electric field versus temperature effects, drift, and threshold voltage phenomena [10], [11].

A previous study focused on thermal characterization of chalcogenides proposed a microthermal stage (MTS) [12]. This structure used either a top platinum (Pt) heater for the thermal actuation of a lateral $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) device or a Pt heater surrounding the GST. The MTS enabled microseconds and even submicroseconds thermal probing. This MTS was able to heat up to 700°C with a thermal time constant of 100 ns. In [11] and [13], another MTS embedded in a vertical PCM mushroom-type memory cell was used to predict changes in the thermal conductivity or thickness of the nearby phase-change layers. In both cases, the MTS was used as a local heater but was not used to melt-quench the PCM because of its relatively long thermal time constant, which prevents the fast cooling times required for amorphization. Therefore, this approach is not suitable for electrothermal characterization within nanosecond (ns) temporal resolution.

Four-terminal, inline, indirectly heated phase-change switches (IPCSs) have been proposed for high-performance RF applications, due to their state-of-the-art figure of merit ($\text{FOM} = 1/(2\pi R_{\text{ON}}C_{\text{OFF}})$) [5]–[8], [14], where R_{ON} is the ON-resistance and C_{OFF} is the parasitic OFF-capacitance. A typical IPCS consists of two RF ports inline with the PCM, separated by a small gap, and two terminals for thermal actuation using an embedded heater. The heater runs transversely to the direction of the RF path, under the PCM and electrically isolated by a dielectric (e.g., Si_3N_4). The heater in the IPCS can induce rapid heating rates [15] and can, therefore, not only set (crystallize) the PCM but also reset (amorphized by melt quench) the chalcogenide material.

In this article, we report on the use of IPCS device structure as a platform for electrothermal characterization of phase

transition properties of PCM in nanoscale films at ns temporal resolution. The heater–thermometer and the PCM are separated vertically by a thin dielectric layer, whose thickness is determined by thin-film deposition (e.g., sputtering), in contrast to lateral separation which is limited by lithography. The isolation between the heater and the PCM layer electrically decouples the heating pulse and PCM probing. Thus, by applying simultaneously a programming pulse to the heater and a reading pulse to the PCM path, the phase transition, as well as temperature-dependent properties up to temperatures of ~ 1100 K, can be measured during a heating pulse, with ns resolution. Furthermore, this novel technique allows to track the temperature of the heater by probing its resistance.

We use GeTe as a prototype material with known physical properties (e.g., melting temperature and crystallization kinetics) [16] and known processing methodologies (e.g., surface treatment for low ohmic contacts [17], [18]). Measurements are carried out using RF probes for the heater to reduce the overshoot and ringing of short pulses and produce clean waveforms for ns probing. Overall, our platform can be used to uncover the intriguing kinetics of crystallization and amorphization in chalcogenides (e.g., GST and SbTe) and other amorphous semiconductors, critical to improve the performance and reliability of phase-change memory for storage and other applications. Furthermore, since the heater is buried underneath the PCM, our setup allows for scanning probe measurements of the PCM top surface. We carry out temperature mapping of the PCM by scanning thermal microscopy (SThM) from the top surface. The SThM signal is calibrated using finite-element method (FEM) simulations in COMSOL Multiphysics and electrothermal measurements of the heater [7].

This article is organized as follows. In Section II, we introduce the IPCS working principle, structure, and our fabrication process. In Section III, we describe the experimental setup that allows for ns probing of the phase transition using the IPCS. Experimental results are presented in Section IV, including electrical thermometry of the heater, the novel two-pulse measurement, and SThM scanning of the IPCS. Finally, this article is summarized in Section V.

II. FOUR-TERMINAL, INLINE, INDIRECTLY HEATED PHASE-CHANGE SWITCH

The IPCS consists of a PCM connected inline by two ports (P_1 and P_2), thermally activated from beneath by an embedded microheater. The heater is electrically isolated from the PCM by a dielectric material (e.g., Si_3N_4 or AlN) [8]. Thus, the programming (actuation) path and the reading paths are electrically decoupled. A cross section and optical view of the IPCS is shown in Fig. 1. The PCM layer is connected inline by two electrodes of width W_{PCM} , separated by a small gap of length L_{Gap} . The PCM layer is thermally activated from beneath by a heater of width W_{H} and length L_{H} . We use GeTe as the prototype PCM due to the extensive prior work done with this material [5]–[9].

To amorphize (reset) the PCM, a narrow width and large amplitude voltage pulse is applied to the heater. Its power must be sufficiently high to raise the temperature of the PCM

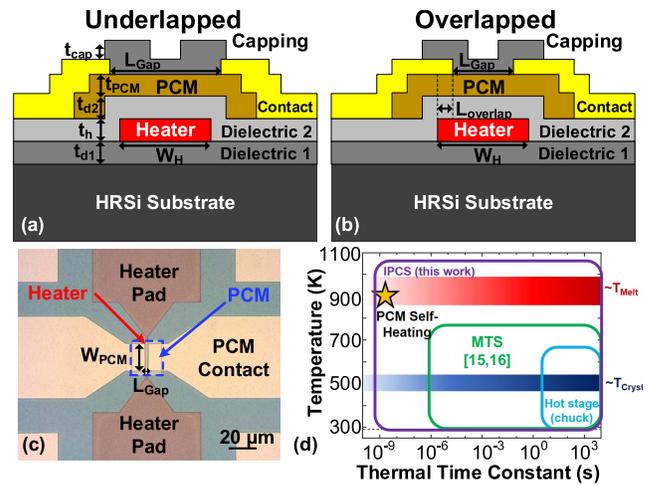


Fig. 1. IPCS device structure and its use as a platform for ns probing of phase transition. Schematic cross section of (a) underlapped and (b) overlapped IPCS device structure. Note in (b) overlap between the contacts and the heater (L_{Overlap}). (c) Top-view optical micrograph of a fabricated IPCS. A PCM is connected inline by two electrodes of width W_{PCM} , separated by a small gap of length L_{Gap} . The PCM layer is thermally activated from beneath by a heater of width W_{H} and length L_{H} . (d) Comparison of thermal time constants and temperature range for different thermal characterization methods of PCM. Our platform allows for thermal characterization with ns time resolution and beyond T_{M} .

above its melting temperature ($T_{\text{M}} \simeq 720$ °C in the case of GeTe). When the pulse is turned off, the quench process begins, quickly cooling the PCM and freezes the material in an amorphous phase (i.e., high resistivity state, $\text{HRS} > 10$ k Ω). To crystallize (set) the PCM to its low resistive state (LRS), a wide pulsewidth and middle amplitude voltage pulse is applied to the heater, thus raising the temperature of the GeTe beyond its crystallization temperature ($T_{\text{Cryst}} \simeq 200$ °C in steady state). The built-in electrical isolation between the PCM path and the heater allows to probe not only the crystallization dynamics as in previous works [11]–[13] but also the melt-quench process, i.e., with temperatures and thermal time constant within the PCM self-heating, as shown in Fig. 1(d).

The switches are fabricated as outlined in [7]. Two different types of samples are used in this study, which differs in the relative position of the PCM contacts with respect to the heater. Fig. 1(a) and (b) shows that the contacts can be overlapped or underlapped. In the first type (underlapped), $W_{\text{H}} = 2$ μm and $L_{\text{Gap}} = 2.2$ μm , whereas in the second type (overlapped), $W_{\text{H}} = 3$ μm and $L_{\text{Gap}} = 1$ μm . Hence, larger capacitive coupling is expected for the latter. Furthermore, due to topographic step changes in the heater area, the underlapped sample suffers from reliability issues, i.e., larger as-deposited R_{ON} and resistance degradation upon cycling. Conversely, when the contacts and the heater are overlapped, R_{ON} is reduced and the reliability improves. The optimal structure in terms of reliability and low capacitive coupling between the heater and the PCM contacts would consist of a planarized IPCS with buried heaters [19] and underlapped contacts.

The two types of samples also differ slightly in the fabrication process. Both samples are fabricated on high-resistivity Si wafers ($\rho > 10$ k $\Omega \cdot \text{cm}$). In the underlapped sample, 100-nm SiO_2 is thermally grown (dielectric 1). Then, W-heaters (120 nm) are sputtered by dc magnetron sputtering. The

heaters are dry-etched using reactive-ion etch (RIE). A 100-nm Si_3N_4 insulating layer (dielectric 2) is then deposited using plasma-enhanced chemical vapor deposition (PECVD). A 100-nm GeTe layer is then dc sputtered from a 50:50 target and heated *in situ* up to 200 °C for 15 min, which is then patterned with RIE. Premetallization surface treatment is performed with descum and deionized water [17]. Ti(20 nm)/Au(200 nm) contacts are e-beam evaporated and patterned by lift-off. After contact deposition, a 100-nm SiO_2 layer is sputtered to passivate the GeTe and patterned using RIE. Vias are opened through the Si_3N_4 to the W-heaters and pads are metallized with Ti/Au (10 nm/100 nm). Finally, the devices are annealed at 220 °C in vacuum. The overlapped sample uses 60 nm of SiO_2 as dielectric 1, Ti/TiN/W (5 nm/30 nm/110 nm) heaters, with 40 nm Si_3N_4 as dielectric 2, and 80 nm GeTe. The remaining steps and layer thicknesses are similar to the other sample.

III. EXPERIMENTAL MEASUREMENT SETUP

The employed measurement setup consists of a Keysight B1500A with high-voltage semiconductor pulse generator units (HV-SPGU) with 50- Ω output resistance and a Keysight Infiniium DSOS804A oscilloscope. Channel 1 (CH1) of the scope is set to high-Z (1 M Ω) input and connected in parallel to the heater ports, as shown in Fig. 2. The heater pads (H_1 and H_2) are probed with ground-signal (GS) RF probes, connected in parallel to the scope and SPGU1 with 2.92-mm coaxial cables and a T-adaptor. Port P_1 is connected to the SPGU2 and P_2 of the IPCS is connected in series to the second channel (CH2) of the scope, which is set to 50- Ω input resistance.

Unlike typical PCM and IPCS measurements reported to date, where the programming and reading pulses are applied separately, here, we apply both pulses simultaneously. A small amplitude, long read pulse is applied to the PCM pads (P_1 and P_2) to monitor its resistance variation, while the programming pulse is applied to the heater. The amplitude of the read pulse is kept low so that it does not induce joule heating in the PCM. The read voltages are 200 and 30 mV for the underlapped and overlapped samples, respectively.

The programming pulses are applied to the heater and they vary in length and width for set and reset. When the voltage pulse is applied to the heater, its temperature (T_H) rises due to the Joule heating. As T_H rises, R_H increases according to its temperature coefficient of resistance (TCR). The heater resistance is given by

$$R_H = 2R_{C_H}/W_H + R_{sh_H}L_H/W_H \quad (1)$$

where R_{C_H} is the contact resistance per width, R_{sh_H} is the sheet resistance, and L_H of the heater. The heater voltage is

$$V_H = 2V_{PG1} \frac{R_H}{R_o + R_H} \quad (2)$$

where V_{PG1} is the voltage applied by the SPGU1 to a 50- Ω load and $R_o = 50 \Omega$ is the output resistance of the SPGU. Changes in R_H will change V_H until a steady-state temperature is reached (few hundred ns). Thus, from the measured voltage at CH1 of the scope (V_{CH1}), which is equal to $V_H(t)$, we

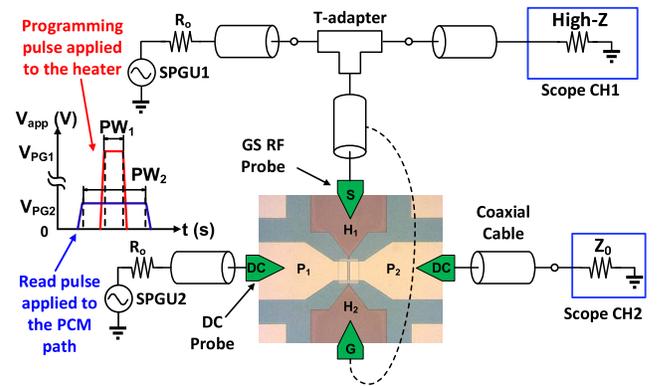


Fig. 2. Measurement setup for simultaneous programming (heating) and reading (probing PCM resistance). The heater pads are connected to SPGU1 and to the scope in high impedance (1 M Ω) in parallel with a T-adaptor, which allows applying programming (heating) pulse and measuring the heater temperature (obtained from its change in resistance). One of the PCM terminals (P_1) is connected to SPGU2, which applies a reading pulse, and the second terminal (P_2) is connected in series to CH2 of the scope in 50 Ω , which measures the changes in R_{PCM} (probe phase transitions) during the heating pulse.

can determine the resistance variation of the heater ($\Delta R_H(t)$). Then, with the TCR, we can infer the temperature variation of the heater ($\Delta T_H(t)$) as

$$\Delta T_H(t) = \frac{\Delta R_H(t)}{R_{sh_H,RT}L_H/W_H \times \text{TCR}} \quad (3)$$

where $R_{sh_H,RT}$ is the sheet resistance of the heater at room temperature (RT). Here, we assume that R_{C_H} does not vary with temperature (as observed in our experiments). The power on the heater is then calculated as $P_H = V_H^2/R_H$.

The TCR of the heater is determined using a transfer-length method (TLM) structure of the heater with widths $W_H = 2$ and 4 μm and lengths L_H from 5 to 30 μm at varying temperatures (from RT to 150 °C in the underlapped sample and from RT to 400 °C in the overlapped sample) using a Linkam thermal stage. The TCR is expected to be constant over the temperature range (up to T_M of the PCM) as shown in [20]. In (3), we assume that: 1) the temperature is uniform along the width of the heater and 2) each part of the heater contributes equally to the resistance change (resistance per length is constant). We revisit these assumptions in Section IV-C.

Our setup allows the measurement of transient PCM voltage $V_{PCM}(t)$ and current $I_{PCM}(t)$. Thus, the transient resistance $R_{PCM}(t)$ can be determined, while the pulse is applied. These electrical measurements are determined from the measured voltage at CH2 (V_{CH2}) of the scope, corresponding to the voltage drop on the 50- Ω input resistance (Z_0). Since the PCM path is connected in series with CH2, $I_{PCM} = V_{CH2}(t)/Z_0$. Then, V_{PCM} is determined as

$$V_{PCM}(t) = 2V_{PG2} - I_{PCM}(t)(R_o + R_s) - V_{CH2}(t). \quad (4)$$

Since $R_o = Z_0$, it follows that:

$$R_{PCM} = 2Z_0 \left(\frac{V_{PG2}}{V_{CH2}} - 1 \right) - R_s \quad (5)$$

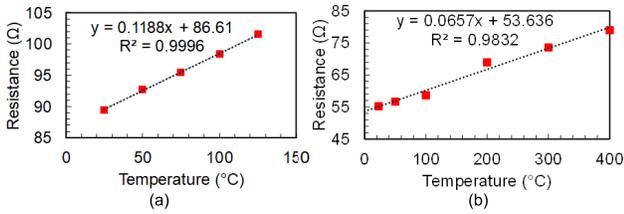


Fig. 3. TCR Extraction. Resistance versus temperature of a 2- μm -wide and 30- μm -long heater. (a) Underlapped sample (120 nm W). (b) Overlapped sample (5-/20-/110-nm Ti/TiN/W).

where V_{PG2} is the voltage applied by the SPGU2 to a 50- Ω load and R_s is the resistance of the PCM pads. Note that R_{PCM} can be measured only, while the read pulse is applied.

IV. EXPERIMENTAL RESULTS

A. TCR Extraction

The TCR is used to convert changes in the electrical resistance of the metal heater to temperature. First, we characterize the temperature dependence of the heater resistance. Fig. 3(a) and (b) shows the temperature-dependent resistance of the W and the Ti/TiN/W heaters, respectively. The TCR of the W-heater and the Ti/TiN/W-heater are, respectively, 0.0013 K^{-1} and 0.0012 K^{-1} . Our experiments show that R_C is independent of temperature, but the specific electrical resistivity of the heater increases linearly with temperature.

B. Two-Pulse Measurements

The devices are probed as explained in Section IV-A, with a temporal resolution of 1 ns. The phase transition can be traced by probing $R_{PCM}(t)$ from V_{CH2} using (5). The temperature variation of the heater, $\Delta T_H(t)$, is determined from V_{CH1} using (3). Since the pulses are synchronized, $R_{PCM}(t)$ can be correlated with $\Delta T_H(t)$, thus helping to understand what is the minimum power required to achieve T_M , T_{cryst} and to calculate the crystallization and quenching times (t_{cryst} and t_{quench} , respectively). Devices are in LRS as-deposited, though the crystalline resistance (R_{cryst}) vary between samples. Amorphization pulses are applied to the pristine devices until the resistance switches to HRS or amorphous phase resistance (R_{amorph}).

The measured $V_H(t)$, $I_{PCM}(t)$, $\Delta T_H(t)$, and $R_{PCM}(t)$ during a partial amorphization process are shown in Fig. 4(a) and (b). The reset pulse is 700-ns-wide and 7.5-V-high ($P = 0.9$ W). Initially, the switch is in LRS, and thus, the current is that of the crystalline phase (I_{cryst}). As the PCM achieves the melting point (after a heating time, $t_{heat} \sim 150$ ns), the resistance reduces below the initial R_{cryst} to the resistance of melted GeTe (R_{melt}). This is in agreement with previous study of GST, which showed that its resistivity at the liquid state is lower than the (RT) crystalline phase [21]. The low liquid state resistance can be explained by the pseudogap model, which predicts the negative TCR in liquid semiconductors [22].

As the pulse ceases, the quenching process is triggered, partially amorphizing the PCM, hence reducing the current to I_{amorph} . Note that the quenching process is relatively slow in these devices due to their large dimensions. A full amorphization process is shown in Fig. 5(a), where a 7.75-V, 700-ns

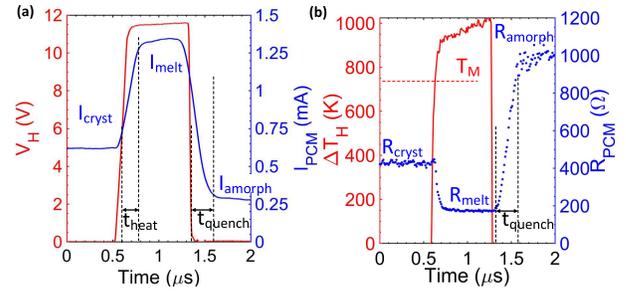


Fig. 4. Simultaneous measurements of the heater and PCM dynamics (underlapped IPCS). (a) Measured transient heater voltage (V_H) and PCM current (I_{PCM}) during a reset pulse of 7.5 V ($P = 0.9$ W). The device is initially in the crystalline state with current I_{cryst} . The PCM heats up and reaches the melting temperature, and thus, the current increases to I_{melt} . When the pulse ceases, the quenching process is triggered, amorphizing the PCM to a higher resistance state (with current I_{amorph}). Note that the heating time (t_{heat}) is approximately equal to the cooling time (t_{quench}). (b) Heater temperature variation (ΔT_H) and transient PCM resistance (R_{PCM}) during the reset pulse in (a). $\Delta T_H(t)$ is extracted from (3), whereas $R_{PCM}(t)$ is obtained from (5). When the PCM reaches the melting temperature, the resistance reduces to R_{melt} , below the resistance in the crystalline phase (R_{cryst}). As the PCM cools down, it partially amorphizes to R_{amorph} .

pulse is applied to the heater ($P = 1$ W). For this sample, the extracted full quenching time is ~ 300 ns ($\tau_{quench} = 135$ ns). This large τ_{quench} is consistent with the large thermal time constant expected in indirectly heated switches [23]. The final state of the device cannot be precisely determined during the transient with our setup since the measured voltage on CH2 is in most cases within the noise floor. Hence, it is measured in dc following the pulse using the Keysight B1500A semiconductor measurement unit (SMU). The final HRS, in this case, was ~ 1.2 M Ω .

The crystallization process is shown in Fig. 5(b) for a 5-V, 900-ns set pulse ($P = 0.4$ W). The estimated T_{cryst} for sub- μm pulses is ~ 350 $^{\circ}\text{C}$, similar to the estimation in [9]. The measured crystallization time is approximately 400 ns, which is shorter than the time reported in [6] and [23] and in our previous work [7]. Using this result, set pulses of 400 ns are used on the overlapped sample, which results in full crystallization [see Fig. 6(a)]. For this sample, pulses of 7 V ($P = 1$ W) are used since the overlapped contacts and the thinner dielectric 1 (SiO_2) reduce the thermal resistance compared with the underlapped sample. Alternatively, the set power can be reduced to 0.8 W when using 6.5-V, 600-ns set pulses due to the higher ΔT obtained at longer pulses [7].

The reset dynamics for the overlapped sample are shown in Fig. 6(b), where pulses of 200 ns and 10.5 V ($P = 2.2$ W) are used. Due to the low R_{ON} and the additional coupling from the overlap capacitance between the PCM contacts and the heater, a coupling effect is observed, while $\Delta T > T_M$. The minimum power for amorphization (MPA) and crystallization (MPC) is consistent with the reported values in [6]. The extracted total quenching time for the overlapped sample is ~ 200 ns ($\tau_{quench} = 90$ ns). Fig. 6(c) shows the transient resistance and ΔT_H when a reset pulse is applied to the device in HRS. It can be observed how the resistance drops, once again, below the resistance of the crystalline state and returns to HRS. A slow fall-time pulse could be used, conversely, to study the melting-to-crystalline transition.

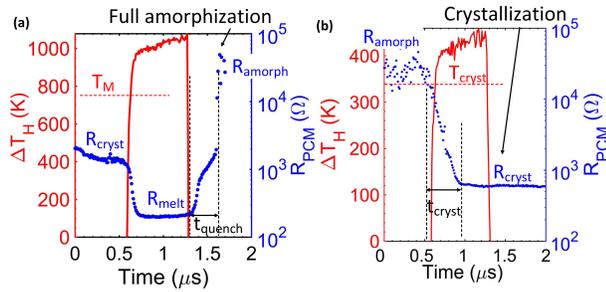


Fig. 5. Phase transition dynamics in underlapped IPCS. (a) Amorphization of the PCM when $P = 1$ W. In this case, the final R_{amorph} is >40 k Ω (beyond noise floor of the scope). (b) Crystallization of the PCM for a pulse with $P = 0.4$ W. Initially, the resistance is at the HRS. When the temperature raises above the crystallization temperature (T_{cryst}), the PCM crystallizes and its resistance is set to the LRS.

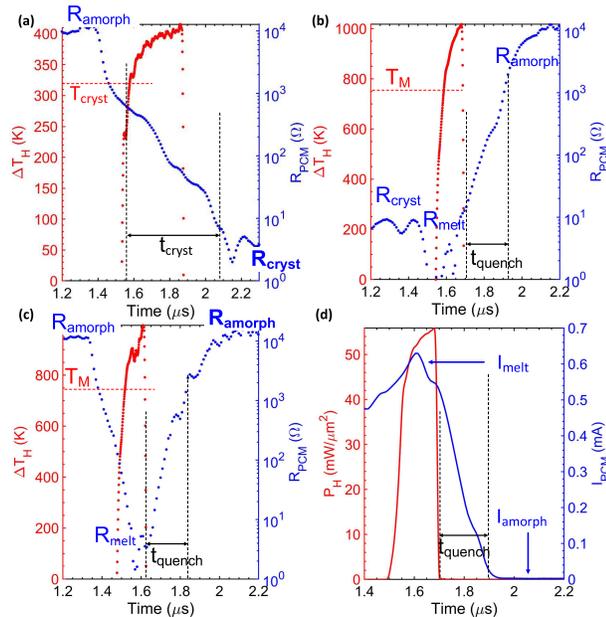


Fig. 6. Phase transition dynamics in overlapped IPCS. Transient ΔT_H and R_{PCM} : (a) during a crystallization process with a 6.5-V, 400-ns pulse. The crystallization process continues after the programming pulse ends because the cooling time is at least 200 ns. (b) Amorphization process with a 10.5-V, 200-ns pulse. In this case, a small coupling is observed between the programming signal and the read pulse. (c) Reset pulse when the IPCS is in the amorphous phase. The resistance reduces below R_{cryst} . (d) Power density and PCM current dynamics. Note how I_{PCM} increases when the PCM reaches T_M and then declines by orders of magnitude as the PCM quenches.

The power density of the heater and the current through the PCM is shown in Fig. 6(d). Both the increased MPA and MPC, and the reduced τ_{quench} in this sample are a result of the reduced thermal resistance (thinner SiO_2 and Si_3N_4 layers, and overlapped contacts). Similarly, the heating and cooling times are shorter than in the underlapped structure. These results are in agreement with previous work [6], [23].

C. Spatially Resolved SThM

We carry out spatially resolved thermometry on underlapped devices by SThM to better understand the heat dissipation in the device. The scans are carried out using an SThM module from Bruker connected to an Asylum MFP-3D Origin atomic force microscope (AFM). The SThM uses a thermoresistive

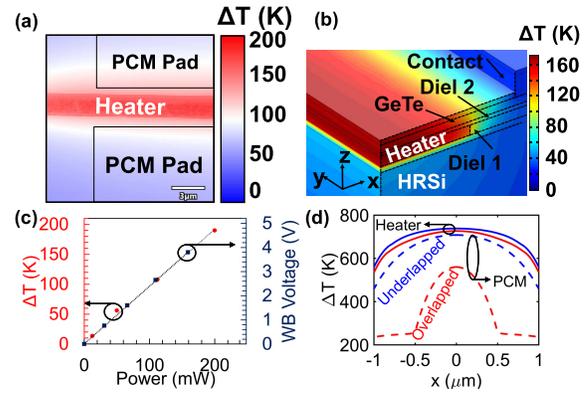


Fig. 7. Spatially resolved thermometry of the IPCS by SThM and Modeling. (a) SThM map of an underlapped IPCS with $W_H = 2$ μm and $W_{\text{PCM}} = 40$ μm for a 5-V bias voltage. Colorbar represents converted ΔT from the measured voltage at the WB in the SThM [see panel (c)]. (b) FEM electrothermal simulation, for the same power bias as in the SThM experiment at steady state. (c) Conversion chart of simulated ΔT (red dots) and SThM WB voltage (blue squares) versus power. (d) Lateral ΔT profile of the heater (solid) and on the top surface of the PCM (dashed) for underlapped (red) and overlapped (blue) devices. The top surface of the PCM is cooler in the overlapped structure (at similar heater temperature) because of heat dissipation to the metal contacts.

probe that works as a nanoscale thermometer. This probe is connected to a Wheatstone bridge (WB) that measures changes in the electrical resistance of the probe as a consequence of variations in its temperature [24]. Under this configuration, a low current flows across the tip to determine its resistance, but it must be sufficiently low to avoid self-heating. In this sensing mode, the tip can obtain simultaneously a topographic and a thermal map of the sample. This technique was used to characterize different types of memory devices [25]–[27].

For the IPCS, we induce local heating in the heater lines by applying a bias voltage to the pads using the probe station of the AFM and a Keithley 4200A semiconductor parameter analyzer (SPA). The thermoresistive probe is first brought in contact with the sample when no voltage is applied to the heater. At this point, the potentiometer of the SThM is adjusted to balance the WB signal. Then, a bias of 0.5 V is applied to the heater pads and the SThM probe is used to obtain thermal maps of the devices. This process is repeated at bias voltages from 1 to 5 V. Additional measurements without bias applied to the heaters are taken in between the steps to warrant that there are no thermal offsets.

The nonflattened thermal profile obtained with the SThM while applying a 5-V dc bias is shown in Fig. 7(a). The SThM signal measured in the bridge increases in proportion to ΔT_H . The heater line shows maximum heating at the center of the line with decay at the edges, as expected. The bridge signal from the SThM probe is calibrated with an FEM electrothermal model of the IPCS for a 5 V stimuli [see Fig. 7(b)]. The obtained conversion factor is 0.027 V/K [see Fig. 7(c)]. ΔT on the top of the passivation layer, above the heater, is approximately 165 K in the SThM scan. The simulated lateral ΔT profile of the heater and the top surface of the PCM is shown in Fig. 7(d). The thermal scanning and our simulations show that, as expected, the maximum ΔT reduces as the PCM electrodes are closer to (or overlapped with) the heater.

V. CONCLUSION

In this work, we presented the IPCS as a novel platform for ns probing of phase transition in thin films. We used GeTe as a prototype chalcogenide PCM in two device types, with underlap and overlap between the heater and PCM contacts. The dynamics of the phase transitions were probed by measuring the electrical resistance of the PCM during crystallization and amorphization. The heater of the IPCS allows for fast heating above the melting temperature of the PCM (>1100 K) while probing the temperature at ns resolution.

We used the IPCS to measure crystallization times of ~ 400 ns at a temperature of 350°C . Cooling times of 200 to 300 ns were measured for the overlapped and underlapped device structures, respectively. We also presented the first direct temperature mapping of an IPCS by SThM from the top surface. The SThM results were calibrated with a 3-D electrothermal FEM model. The obtained temperature maps validated uniform heating by the microheater and showed the effect of lateral heat spreading by the PCM contacts.

The key advantage of our measurement technique is the ability to probe the temperature-dependent dynamics of the phase transition. In conventional two-terminal PCM devices, the transient resistance can be measured, but the local temperature is unknown. The four-terminal IPCS structure allows separating the heating path from the PCM, but thus far, it was used only for “cold” switching, i.e., the PCM resistance was probed before and after, but not during thermal actuation. PCMs are currently being evaluated not only as storage and memory devices but also as neuromorphic hardware and RF switches. Our method can shed new light on the phase transition dynamics and can help select materials, device structures, and programming pulses for such emerging technologies and applications.

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