# Verilog-A model – Y-flash memristive device

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## 1 Characteristics of the model

- The model has more than 650 accurate resistance levels for 50% duty-cycle $20\mu s$ pulse inputs.
- The model captures deterministic memristive dynamics as per the requirement.
- It can be used to design neuromorphic circuits at the schematic-level for simulations and analysis.

## 2 Modeling Methodology

### 2.1 Programming mode (4.5V & 5V)

The Y-flash device characteristics, depending on the programming voltage, can be represented using two models. The long channel model for 4.5V and short channel model for 5V. However, we use the short channel representation to model the device for both the voltages. This is because it is simpler, requires less parameters and is more physically reasonable. The equation of the programming mode in physical parameters ia represented as –

$$\frac{dV_{th}, RESET}{dt} = \frac{I_{inj}}{C_{fr}} = \frac{K'}{C_{fr}}(CR.V_{DS} - V_{th}).P(E_v) \tag{1}$$

Since $K'$ and $CR$ are constants and the variation in $P(E_v)$ is negligible w.r.t. the change in $V_{DS}$, for modeling purposes we take their multiplication as a constant. Along with that, for a specific programming voltage i.e. 4.5V or 5V, the parameter $CR.V_{DS}$ remains constant. Therefore, the equation reduces to –

$$\frac{dV_{th}, RESET}{dt} = b(a - V_{th}) \tag{2}$$

To calculate the equation specific parameters $a$ & $b$, we use the MATLAB curve fitting tool to fit the measured Y-flash data to the fitted equations. The fitted equation is in the form of –

$$V_{th} = a - e^{c-bt} \tag{3}$$

Where $c$ is the integration constant and $t$ is the time period of each pulse input.

Since both the programming voltages are modeled using the short channel model, similar fitted equation constants can be obtained for the other voltage ranges as well, given that the programming data is made available.

Table 1: Fitted parameters for programming voltages 4.5V & 5V

| **Programming Voltage** | ***a*** | ***b*** | **R-squared** |
|---|---|---|---|
| $4.5V$ | 2.16 | $5.1 * 10^{-5}$ | 0.9941 |
| $5V$ | 2.4 | $2.1 * 10^{-4}$ | 0.9952 |

### 2.2 Read mode

The internal state of the Y-flash device can be measured, as resistance, in the sub-threshold region. This is done by providing $2V$ at its terminals and then measuring current across the device.

$$I_{DS} = I_{read}.e^{\frac{CR.V_{DS}}{mV_T}} e^{-\frac{V_{th}}{mV_T}} \tag{4}$$

Where $CR$ & $mV_T$ are constants (subject to definition). The Y-flash memristive device operates in the sub-threshold region in this mode.

### 2.3 Erase mode

We use simulated annealing method to calculate optimized parameters for the data extracted from the measurements to fit in the following equation,

$$\frac{dV_{th}, SET}{dt} = \frac{I_{GIDL}}{C_{dep}} = A.\frac{CR.V_s + V_{ox} - V_{th}}{C_{dep}t_{ox}} e^{-\frac{Bt_{ox}}{CR.V_s + V_{ox} - V_{th}}} \tag{5}$$

By considering $CR.V_S + V_{ox}$ and $\frac{A}{C_{dep}t_{ox}}$ as constants, similar to programming mode, this equation can be reduced to,

$$\frac{dV_{th}, SET}{dt} = a.(b - V_{th})e^{-\frac{c}{b - V_{th}}} \tag{6}$$

Simulation results give us the values of $a$,$b$ and $c$ as,
$a = 4.643 * 10^{-4}$
$b = 0.9531$
$c = 0.07$

Table 2: Model parameters accessible from the Schematic window GUI

| Sno. | Parameter name | Definition | Default value |
|---|---|---|---|
| 1. | CRprog | Coupling ratio for the programming mode equation | 0.48 |
| 2. | Vth_init | User-defined value of the initial threshold voltage | $1V$ |
| 3. | K_Cfr_45, K_Cfr_5 | Constants b as defined in the programming mode equation for 4.5V and 5V | $5.4 * 10^{-5}$, $2.1 * 10^{-4}$ |
| 4. | mVT | Technology constant m times VT (0.026V) | 0.144765 |
| 5. | CR | Constant for the subthreshold region equation (pre-defined) | 1 |
| 6. | Iread | Read current when Vth = 1V | $1 * 10^{-9}$ |
| 7. | resolution | Regulates minimum step size | 1 |

# 3 Operation

## 3.1 Simulation

The reader may note a few important points while performing simulations using the model.

- The state variable $V_{th}$ is bounded between $[1V, 2V]$.
- The parameter **resolution** is given a default value of 1 which translates to a minimum step value of $1\mu s$ (resolution*$1\mu s$). To make the time step of each iteration smaller, say $1ns$, the user can change the resolution to 0.001 & thus can set the step size as $1ns$ (resolution*$1\mu s$).

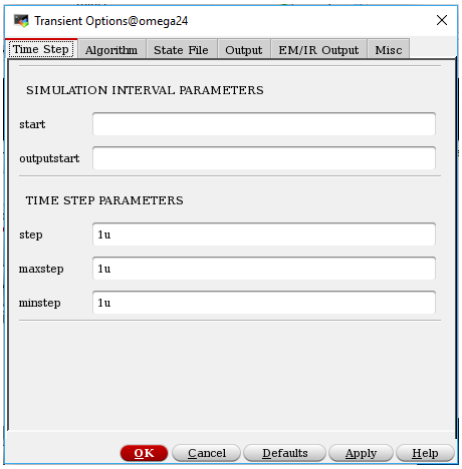



Figure 1: Providing a step size of $1\mu s$ for resolution = 1

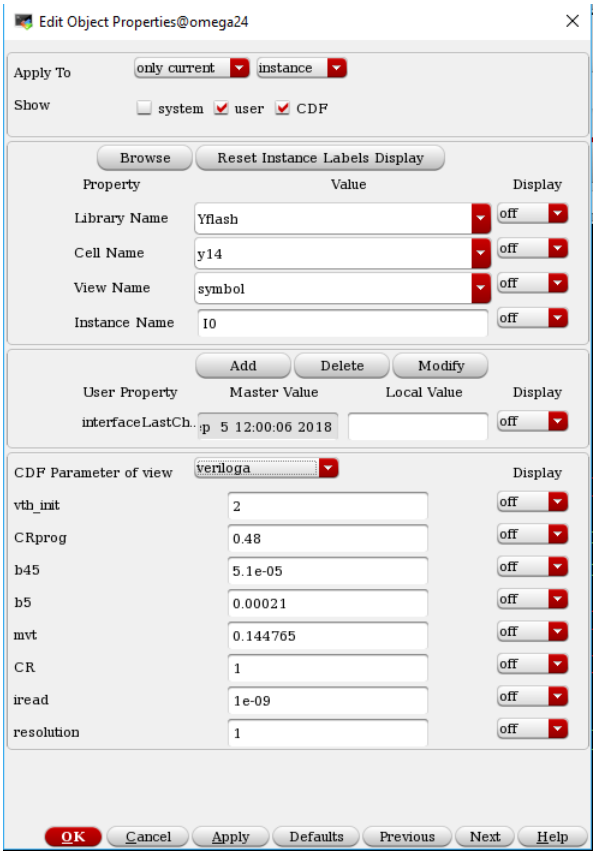



Figure 2: Varying the resolution value from ADEL window

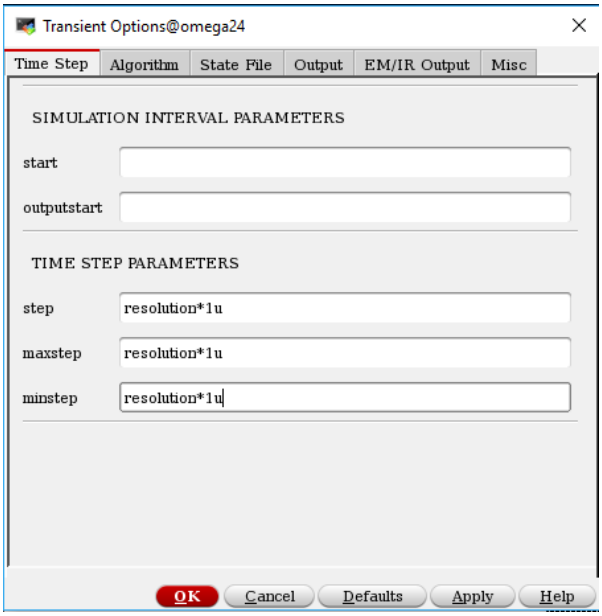
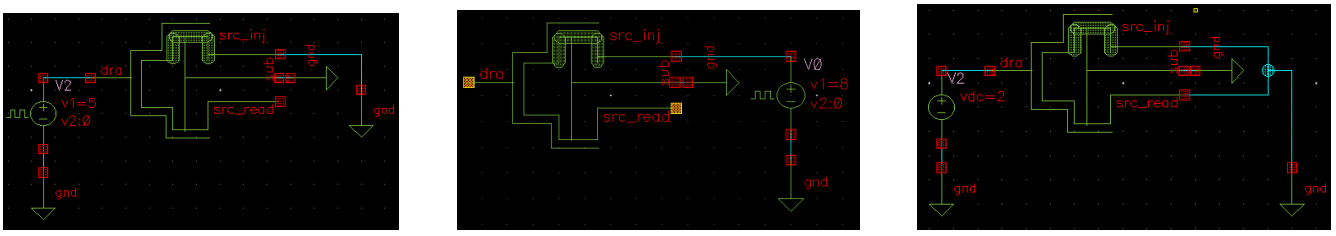



Figure 3: Varying the time-step values accordingly

### 3.2 Schematic connections for different modes

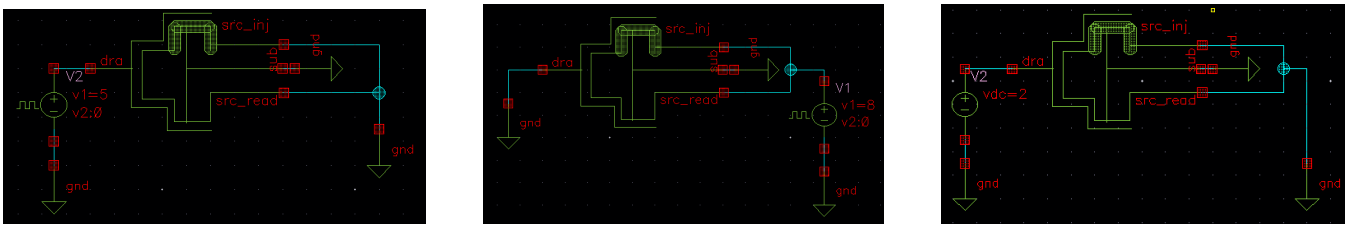
For the Y-flash device to be operated in an array, the user must make connections as per the following.




(a) Programming mode (b) Erase mode (c) Read mode

Figure 4: Circuit connections for operating the model(in an **array**)

For a single Y-flash based memristor cell, the user must make connections as per the following.

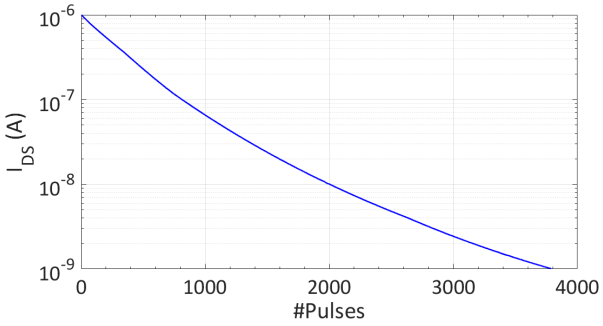



(a) Programming mode (b) Erase mode (c) Read mode

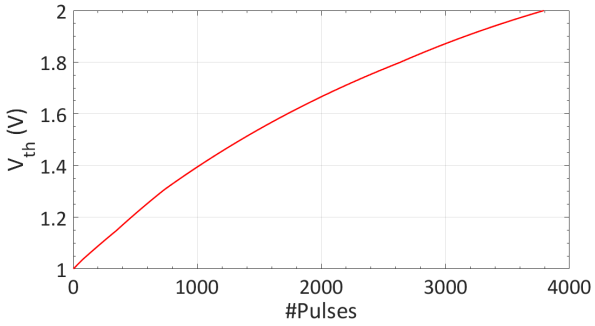
Figure 5: Circuit connections for operating the model(as a **single-cell**)

# 4 Simulation results

## 4.1 5V Programming mode



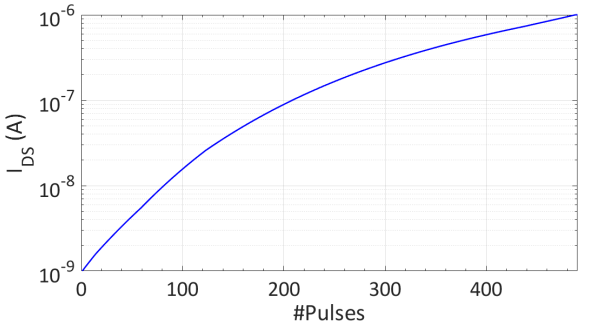

(a) $I_{DS}$ vs #Pulses



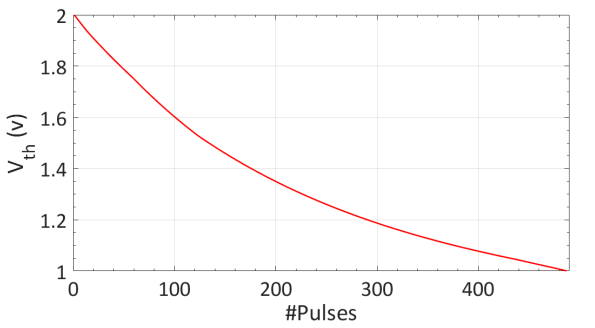

(b) $V_{th}$ vs #Pulses

Figure 6: For 5V programming pulses

## 4.2 8V Erasing mode




(a) $I_{DS}$ vs #Pulses




(b) $V_{th}$ vs #Pulses

Figure 7: For 8V erasing pulses

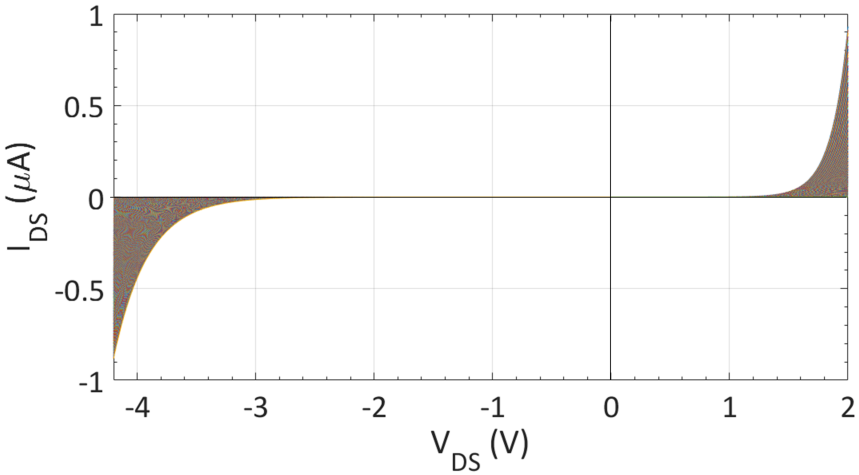



Figure 8: I/V curve for a Y-flash memristive device generated using the model

# 5 Y-flash Verilog – A code

```
`include "constants.vams"
`include "disciplines.vams"

module yflash( src_read, src_inj, sub, dra);
inout  src_read, src_inj, dra, sub;
electrical src_inj, src_read, dra, sub;
ground gnd;

parameter real vth_init = 1;
parameter real CRprog = 0.48;
parameter real K_Cfr_45 = 5.1e-5;
parameter real K_Cfr_5 = 2.1e-4;
parameter real mvt = 0.144765;
parameter real CR = 1;
parameter real iread = 1e-9;
parameter real resolution = 1;

real vth;
real dvthdt;
real first_iter = 0;
real i;

analog begin
if(first_iter==0) begin
        vth = vth_init;
        first_iter = 1;
end

if(V(dra,src_read) <= 2.0) begin
        i = iread*exp((CR*(V(dra,src_read)))/(mvt))*exp(-vth/mvt);
        dvthdt = 0;
        I(dra) <+ i;
        I(src_read) <+ -i;
end

if (V(dra,src_inj)== 4.5) begin
        dvthdt = K_Cfr_45*(CRprog*V(dra,src_inj) - vth);
        I(dra, src_inj) <+ 0;
end

if (V(dra,src_inj) == 5) begin
        dvthdt = K_Cfr_5*(CRprog*V(dra,src_inj) - vth);
        I(dra, src_inj) <+ 0;
end

if (V(src_inj,gnd) == 8) begin
        dvthdt = 4.643e-4*(0.9531-vth)*exp((-0.07)/(0.9531-vth));
end

if(vth < 1.0 || vth > 2.0)begin
        dvthdt = 0;
end

vth = vth + resolution*dvthdt;

I(sub) <+ 0;
dvthdt = 0;
end

endmodule
```