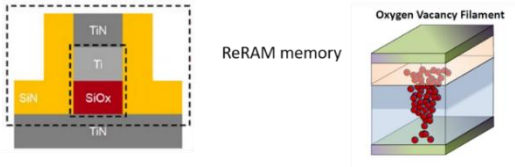
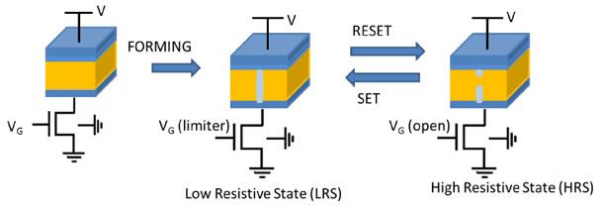
ASIC² ARCHITECTURES SYSTEMS INTELLIGENT COMPUTING INTEGRATED CIRCUITS

# Weebit ReRAM Characterization & Modeling

Resistive Random-Access-Memory (ReRAM) is a very promising technology for Non-Volatile Memory (NVM), especially at the smaller process geometries. ReRAM is orders of magnitude faster and lower power consumption compared to Flash memories.




Weebit, incorporated in Israel in 2015, addresses the growing need for data storage and NVM technology with its new, ReRAM technology. Weebit's ReRAM cell consists of 2 metal layers with a Silicon Oxide (SiOx) layer between them. In an initial, one-time, forming step, positive voltage is applied on the cell to form a conductive filament, and entering a Low Resistive State (LRS). After that – applying negative voltage can break the filament, moving to a High Resistive State (HRS), and positive and negative voltages can cause the cell to move from one state to the other.




In this project, Weebit's 8x8 1T1R ReRAM array samples will be characterized and evaluated. ASIC² lab infrastructure will be used to test the switching capabilities of Weebit's devices, including: switching time, HRS/LRS ratio, I-V curve, and endurance. Then, a Verilog-a device model will be fitted to the measured data. Finally, the fitted model will be used to simulate the devices in a large crossbar array.

## Project Schedule:

- Learn about ReRAM and Weebit's device features.
- Learn about ASIC² Python-based lab infrastructure.
- Using the lab infrastructure, characterize Weebit's 1T1R device and array.
- Fit the characterized device to a Verilog-A model.
- Simulate the device in a large crossbar array using Virtuoso (Cadence).

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Prerequisite: LAB1 (part 1 and two)