Sub-Nanosecond Pulses Enable Partial Reset for Analog Phase Change Memory

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Abstract—A key bottleneck in using phase change memory (PCM) for training artificial neural networks is the abrupt nature of the melt-quench process (amorphization), which does not allow gradual reset. Here we demonstrate analog reset (partial amorphization) in PCM by applying sub-nanosecond programming pulses. Intermediate-level reset states are enabled by reducing the pulse width below the dominant thermal time constant of the PCM, which is on the order of a few nanoseconds. We show gradual change in PCM resistance as a function of number of (sub-ns) reset pulses with 50 intermediate states. Our unique scheme allows fine-tuning the resistance with sub-ns pulses of constant amplitude, which can significantly reduce the programming complexity in training neuromorphic hardware.

Index Terms— Analog PCM, Partial Reset, Sub-ns Pulses, Multi-level PCM, Neuromorphic Devices, Resistance Drift

I. INTRODUCTION

Phase change memory (PCM) has matured as a storage class memory, and is more recently being evaluated for neuromorphic hardware [1–3]. PCM relies on the large resistivity contrast between the crystalline (low resistive state, LRS) and amorphous (high resistive state, HRS) phases in chalcogenide compounds, such as Ge₂Sb₂Te₅ (GST). The phase transition is induced thermally using electrical pulses of crystallization (set) and amorphization (reset) [2].

In neuromorphic applications, synapses are important building blocks. With their adjustable conductance, PCM devices can store (and train) weights of the neural network, and efficiently implement the vector-matrix multiplication required for artificial neural networks [1,4–6]. This requires analog-type behavior i.e., a gradual change in resistance. However, the amorphization in PCM is based on a melt-quench process which typically results in abrupt reset, i.e. a sharp resistance change. Previous studies therefore tuned PCM resistance by partial crystallization (set only) [7–12], by applying reset pulses with varying amplitude [9,13,14], or by using special structures and initialization steps [15], which significantly increases programming complexity.

In this work, we show that partial amorphization (analog reset of PCM), which allows for bi-directional weight update, can be achieved with constant amplitude, sub-nanosecond (ns) pulses, without initialization or dedicated cell structures. Analog reset behavior is enabled using pulse widths (PWs) shorter than the thermal time constant of the device \( t_\text{th} \). We also characterize \( t_\text{th} \) by dynamic measurements of the transient resistance and show that it is in the range of \( \sim 1-3 \) ns in our devices (via diameter \( \sim 100-200 \) nm). Our technique can be used in any PCM cell structure. We envision that the presented method and results can advance the implementation of PCM technology for future neuromorphic applications.

II. HIGH-SPEED MEASUREMENT SETUP AND CONFINED-CELL PCM DEVICES

We used conventional PCM cells of confined GST, fabricated as outlined below, and utilized a high-speed measurement setup, including transmission lines for the access pads to carry out sub-ns programming. The high-speed measurement setup (Fig. 1a) consists of a fast pulse generator (PG) connected in series with the PCM device and a current analyzer. Ground-signal (GS) transmission lines matched to 50 Ω are used to connect the device with the measurement equipment. The output impedance of the PG, as well as the input impedance of the current analyzer are also set to 50 Ω.

The focused ion beam (FIB) scanning electron microscope (SEM) cross-section of a confined PCM cell is shown in Fig. 1b, fabricated as follows [16]. First, tungsten (W) was evaporated, patterned, and etched to form the bottom electrode (BE). Next, SiO₂ was deposited using plasma enhanced chemical vapor deposition (PECVD) and the confined vias were patterned using electron-beam lithography. Sputtering and lift-off were used to pattern the GST layer with TiN capping as well as the final TiN/Pt top electrode (TE) and contact pads. We also carried out an in situ Ar clean prior to GST sputtering, to remove oxidation of the TE and prevent filamentary formation.

The devices are initially set to their LRS, and partial reset (Fig. 1c) is achieved by applying short pulses. The resistance state is read at low voltage (0.1 V) after each pulse as shown schematically in Fig. 1a. This way, gradual reset, as opposed to abrupt switching, is achieved (see Fig. 1c). The gradual change in the volume of the amorphous phase is schematically illustrated in Fig. 1d. The full range of resistance obtained in
The thermal time constant of the device ($\tau_{th}$) is in the range of ~1-3 ns for our devices (Fig. 2a inset). This $\tau_{th}$ corresponds to the time it takes a critical volume of GST to reach the melting temperature [17]. It can be evaluated for a given material, device structure, and GST volume by the product of the thermal resistance and heat capacitance in a simplified lumped model $R_{th}C_{th}$; the specific heat capacity of GST is $c_{GST} \approx 1.3 \text{ J/cm}^3/\text{K}$ [18], and $R_{th}$ could be dominated by interfaces (thermal boundary resistance, TBR $\approx 30 \text{ m}^2/\text{K GW}$ [19]). Here the GST thickness is ~50 nm and the via diameter is ~50 nm and is reduced below the thermal time constant ($\tau_{th} \approx 1-3$ ns, see panel a inset) reset pulses achieve partial amorphization, exhibiting intermediate resistance states and analog reset. Results are shown for device with via diameter of 175 nm. Abrupt reset is shown for comparison in (d) at higher applied voltage (red).

Our partial amorphization scheme is enabled by pulses shorter than the thermal time constant of the device ($\tau_{th}$). We characterized the dominant $\tau_{th}$ experimentally by dynamic measurements of the transient resistance and found that it is in the range of ~1-3 ns for our devices (Fig. 2a inset). This $\tau_{th}$ corresponds to the time it takes a critical volume of GST to reach the melting temperature [17]. It can be evaluated for a given material, device structure, and GST volume by the product of the thermal resistance and heat capacitance in a simplified lumped model $R_{th}C_{th}$; the specific heat capacity of GST is $c_{GST} \approx 1.3 \text{ J/cm}^3/\text{K}$ [18], and $R_{th}$ could be dominated by interfaces (thermal boundary resistance, TBR $\approx 30 \text{ m}^2/\text{K GW}$ [19]). Here the GST thickness is ~50 nm and the via diameter is ~50 nm and is reduced below the thermal time constant ($\tau_{th} \approx 1-3$ ns, see panel a inset) reset pulses achieve partial amorphization, exhibiting intermediate resistance states and analog reset. Results are shown for device with via diameter of 175 nm. Abrupt reset is shown for comparison in (d) at higher applied voltage (red).

III. RESULTS AND DISCUSSION

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(1.7V 2.3V)

Fig. 2. Gradual reset with sub-ns pulses shown by read resistance vs. pulse number for varying reset pulse width: (a) 40 ns, (b) 5 ns, (c) 1 ns, (d) 0.4 ns. As the PW is reduced below the thermal time constant ($\tau_{th} \approx 1-3$ ns, see panel a inset) reset pulses achieve partial amorphization, exhibiting intermediate resistance states and analog reset. Results are shown for device with via diameter of 175 nm. Abrupt reset is shown for comparison in (d) at higher applied voltage (red).
To better understand the nature of the obtained multilevel states we perform electrical analysis, including threshold voltage characterization, and resistance vs. temperature measurements up to the crystalization temperature. We measured the threshold voltage for different intermediate states because it can represent the change in the amorphous volume due to fixed electric field at the threshold point [23], and because the Ovonic threshold switching phenomenon is a unique signature of amorphous chalcogenide semiconductors [24].

Current vs. voltage ($I$-$V$) curves for different states are shown in Fig. 3a. The increasing threshold voltage, from $-0.2$ to $\sim 0.8$ V illustrates the presence of a mixed crystalline-amorphous phase, with increasing amorphous volume corresponding to higher resistance. In addition, the temperature-dependent resistance of intermediates states (Fig. 3b-d) show an increase in the (negative) temperature coefficient of resistance (TCR) at higher resistance states, and a drop in the resistance at the crystallization temperature to the fcc phase ($\sim 450$ K) indicating presence of partial amorphization rather than mixed fcc-hexagonal phase.

Finally, we explore the effect of resistance drift on our sub-ns analog reset scheme. This is an important phenomenon to investigate because it can severely limit the accuracy of conductance tuning, depending on the timescale of the training. In this test, we perform read operations after five programming pulses in time steps of 1.5 s, 10 s, and 100 s (see Fig. 4). Drift becomes more prominent at higher resistance states, as expected, owing to larger volume of amorphous phase [21–24].

Interestingly, the drift effect is “erased” by the subsequent reset pulses. This is shown in Fig. 4b, where the resistance state after a drift measurement (color markers in Fig. 4b) continues from the previous non-drifted state (gray) rather than the “drifted state” (red marker). It should also be noted that a critical conduction path in the PCM must melt to achieve re-amorphization, because heating the material to its melting temperature requires high current and low (transient) resistance. We therefore attribute the gradual change in amorphous volume with increasing number of pulses to the dependence of the melted volume on the initial electrical and thermal resistance of the PCM cell. At constant pulse amplitude, the pulse width must be sufficiently short to allow for such fine control of the obtained amorphous volume and the resulting electrical and thermal resistance. Future work should focus on bi-directional weight update (including potentiation) and improving the precision.

IV. CONCLUSION

We used sub-nanosecond pulse-width programming scheme to demonstrate analog type reset in PCM. This unique behavior, which is essential for neuromorphic applications, is enabled by pulses shorter than the thermal time constant of a critical PCM volume (here $\sim 1-3$ ns). The presented method and results can advance the implementation of PCM technology for future neuromorphic applications, and can help enable training with PCM-based artificial intelligence (AI) hardware.
REFERENCES


