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Sub-Nanosecond Pulses Enable Partial Reset for Analog Phase Change Memory

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***Abstract*—A key bottleneck in using phase change memory (PCM) for training artificial neural networks is the abrupt nature of the melt-quench process (amorphization), which does not allow gradual reset. Here we demonstrate analog reset (partial amorphization) in PCM by applying sub-nanosecond programming pulses. Intermediate-level reset states are enabled by reducing the pulse width below the dominant thermal time constant of the PCM, which is on the order of a few nanoseconds. We show gradual change in PCM resistance as a function of number of (sub-ns) reset pulses with 50 intermediate states. Our unique scheme allows fine-tuning the resistance with sub-ns pulses of constant amplitude, which can significantly reduce the programming complexity in training neuromorphic hardware.**

***Index Terms*— Analog PCM, Partial Reset, Sub-ns Pulses, Multi-level PCM, Neuromorphic Devices, Resistance Drift**

I. Introduction

PHASE change memory (PCM) has matured as a storage class memory, and is more recently being evaluated for neuromorphic hardware [1-3]. PCM relies on the large resistivity contrast between the crystalline (low resistive state, LRS) and amorphous (high resistive state, HRS) phases in chalcogenide compounds, such as $Ge_2Sb_2Te_5$ (GST). The phase transition is induced thermally using electrical pulses of crystallization (set) and amorphization (reset) [2].

In neuromorphic applications, synapses are important building blocks. With their adjustable conductance, PCM devices can store (and train) weights of the neural network, and efficiently implement the vector-matrix multiplication required for artificial neural networks [1,4–6]. This requires analog-type behavior *i.e.*, a gradual change in resistance. However, the amorphization in PCM is based on a melt-quench process which typically results in abrupt reset, *i.e.* a sharp resistance change. Previous studies therefore tuned PCM resistance by partial crystallization (set only) [7–12], by applying reset pulses with varying amplitude [9,13,14], or by using special structures and initialization steps [15], which significantly increases programming complexity.

In this work, we show that partial amorphization (analog reset of PCM), which allows for bi-directional weight update, can be achieved with constant amplitude, sub-nanosecond (ns) pulses, without initialization or dedicated cell structures. Analog reset behavior is enabled using pulse widths (PWs) shorter than the thermal time constant of the device (τ_{th}). We also characterize τ_{th}, by dynamic measurements of the transient resistance and show that is in the range of ~1-3 ns in our devices (via diameter ~100-200 nm). Our technique can be used in any PCM cell structure. We envision that the presented method and results can advance the implementation of PCM technology for future neuromorphic applications.

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II. High-Speed Measurement Setup and Confined-Cell PCM Devices

We used conventional PCM cells of confined GST, fabricated as outlined below, and utilized a high-speed measurement setup, including transmission lines for the access pads to carry out sub-ns programming. The high-speed measurement setup (Fig. 1a) consists of a fast pulse generator (PG) connected in series with the PCM device and a current analyzer. Ground-signal (GS) transmission lines matched to 50 Ω are used to connect the device with the measurement equipment. The output impedance of the PG, as well as the input impedance of the current analyzer are also set to 50 Ω.

The focused ion beam (FIB) scanning electron microscope (SEM) cross-section of a confined PCM cell is shown in Fig. 1b, fabricated as follows [16]. First, tungsten (W) was evaporated, patterned, and etched to form the bottom electrode (BE). Next, SiO_x was deposited using plasma enhanced chemical vapor deposition (PECVD) and the confined vias were patterned using electron-beam lithography. Sputtering and lift-off were used to pattern the GST layer with TiN capping as well as the final TiN/Pt top electrode (TE) and contact pads. We also carried out an *in situ* Ar clean prior to GST sputtering, to remove oxidation of the TE and prevent filamentary formation.

The devices are initially set to their LRS, and partial reset (Fig. 1c) is achieved by applying short pulses. The resistance state is read at low voltage (0.1 V) after each pulse as shown schematically in Fig. 1a. This way, gradual reset, as opposed to abrupt switching, is achieved (see Fig. 1c). The gradual change in the volume of the amorphous phase is schematically illustrated in Fig. 1d. The full range of resistance obtained in

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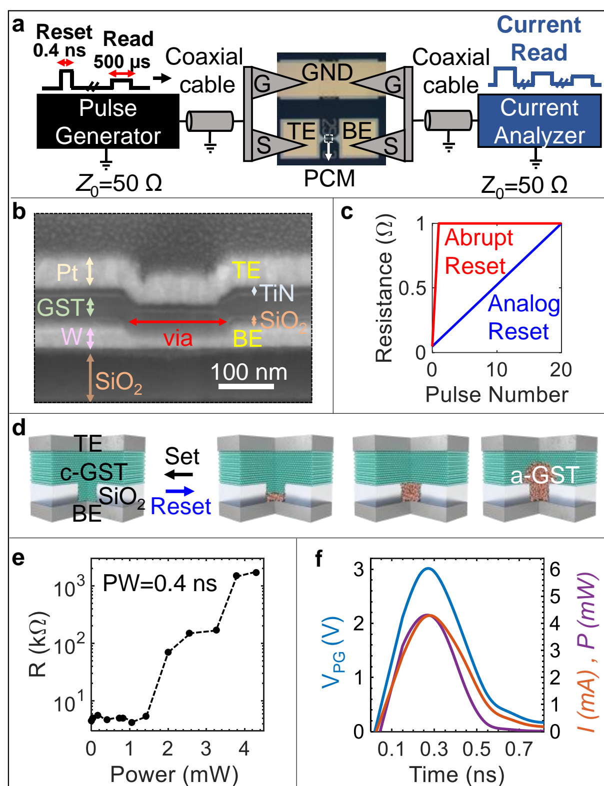

Fig. 1. (a) High speed setup and schematic of the sequential program and read pulses, including transmission lines and ground-signal (GS) probes for minimizing parasitic capacitance effects. (b) Cross section FIB-SEM of the confined GST PCM device. GST is confined in a via-hole (marked by the red arrow) in SiO_2 with varying diameter in the range ~100-200 nm. (c) Schematic illustration of typical PCM abrupt reset (red) *vs.* the analog gradual reset desired for neuromorphic devices (blue). Schematic of the sequential program and read pulses. (d) Illustration of a gradual formation of amorphous volume for sub-ns reset. The concept is demonstrated here for confined cells, but it is also valid for mushroom cells and other PCM device structures. (e) Resistance *vs.* applied reset power at 0.4 ns PW. Before each reset pulse the PCM was set to an initial state of ~1-3 kΩ. (f) Transient waveform of a 0.4 ns reset pulse: applied voltage (blue), measured current (orange) and power (purple).

our devices is shown in Fig. 1e, and the transient waveform of a 0.4 ns reset pulse is displayed in Fig. 1f.

III. Results and Discussion

Our partial amorphization scheme is enabled by pulses shorter than the thermal time constant of the device (τ_{th}). We characterized the dominant τ_{th} experimentally by dynamic measurements of the transient resistance and found that it is in the range of ~1-3 ns for our devices (Fig. 2a inset). This τ_{th} corresponds to the time it takes a critical volume of GST to reach the melting temperature [17]. It can be evaluated for a given material, device structure, and GST volume by the product of the thermal resistance and heat capacitance in a simplified lumped model $R_{th}\cdot C_{th}$; the specific heat capacity of GST is c_{GST}~1.3 J/cm^3/K [18], and R_{th} could be dominated by interfaces (thermal boundary resistance, TBR~30 m^{2}K/GW [19]). Here the GST thickness is ~50 nm and the via diameter

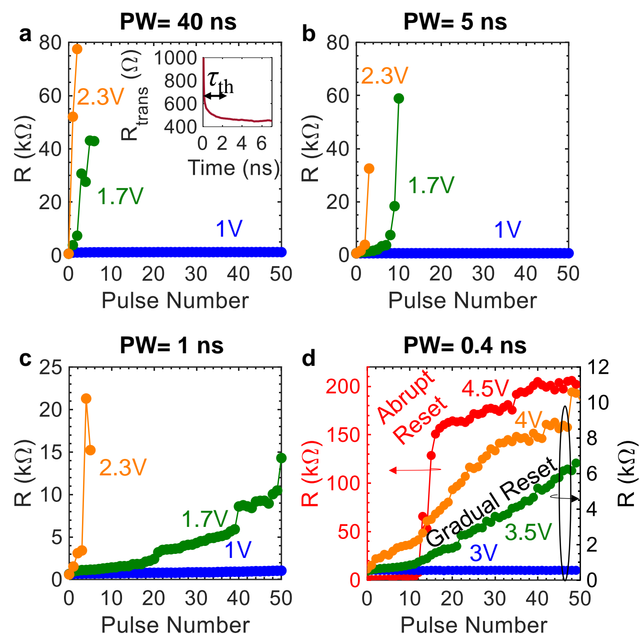

Fig. 2. Gradual reset with sub-ns pulses shown by read resistance *vs.* pulse number for varying reset pulse width: (a) 40 ns, (b) 5 ns, (c) 1 ns, (d) 0.4 ns. As the PW is reduced below the thermal time constant (τ_{th} ~ 1-3 ns, see panel a inset) reset pulses achieve partial amorphization, exhibiting intermediate resistance states and analog reset. Results are shown for device with via diameter of 175 nm. Abrupt reset is shown for comparison in (d) at higher applied voltage (red).

(Fig. 1b) varies between ~100 and 200 nm. In the simple expression given here $\tau_{th}\approx$ 2 ns, considering R_{th}=TBR/A and $C_{th}=c_{GST}\cdot V$, where A is the confined area and V is the GST volume.

The key results of our partial reset experiment are summarized in Fig. 2, showing the evolution of the (read) resistance *vs.* programming pulse number with varying PWs: (a) 40 ns, much longer than τ_{th}, (b) 5 ns, marginally longer than τ_{th}, (c) 1 ns, comparable to τ_{th}, and (d) 0.3 ns, shorter than τ_{th}. Evidently, as the PW is reduced below τ_{th} more intermediate resistance states are achieved, and the reset becomes more gradual. Overall, Fig. 2d shows ~50 intermediate resistance states in the range of ~0.5 kΩ to ~9 kΩ with nearly linear dependence on number of pulses. This is our main finding and it should be emphasized that such intermediate states were obtained to date only by partial crystallization (set) [7–12], or by varying reset pulse amplitude [9], [13,14].

Fig. 2 presents results for devices with via diameter size of 175 nm, but devices with nominal via diameter sizes in the range ~100-200 nm were also measured, exhibiting similar behavior. For a given pulse voltage amplitude, the resistance saturates after a certain number of pulses (*e.g.*, orange markers beyond pulse number 30 in Fig. 2d). We note that the resistance range is lower for shorter PWs, yet it preserves an off/on ratio of nearly 20× and for neuromorphic applications the requirement for analog behavior can outweigh a larger dynamic range [20,21]. Pulses shorter than τ_{th} may require higher power (P), but the energy consumption (E ~ $P\cdot$PW) is not increased because the pulse duration is shorter [22]. Moreover, the alternative method to gradually increase the PCM resistance to an intermediate state (depression) is by first

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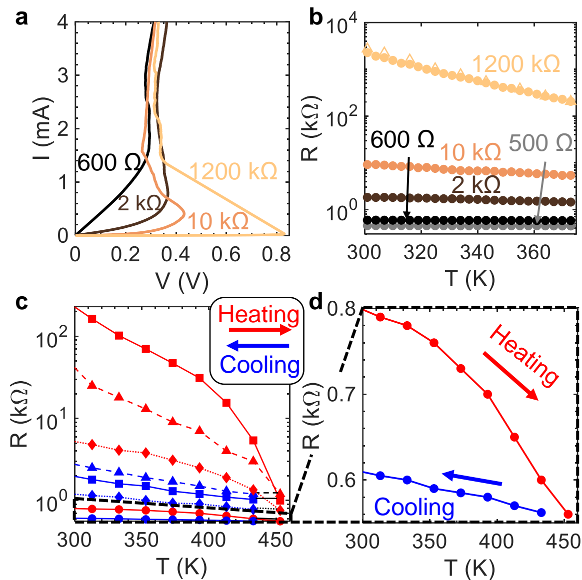

Fig. 3. (a) Current-voltage characteristics of various intermediate resistance states showing the threshold voltage increases with the resistance, corresponding to larger amorphous volume. (b) Temperature-dependent PCM resistance in a limited range below the crystallization temperature for different intermediate states. 500 Ω is considered fully crystalline and 1200 kΩ is considered fully amorphous. Circles represent heating and rectangles represent cooling, which was measured to ensure no phase transition occurred. The amorphous phase has a large negative TCR, fcc has low negative TCR, and hcp has near zero TCR. (c) Non-volatile decrease of resistance upon heating to the (fcc) crystallization temperature (~450 K) of different intermediate resistance states, indicating phase transition from amorphous to fcc. Each shape represents different initial reset state. Red and blue colors for heating and cooling, respectively. (d) Zoomed in plot of the transition temperature for low resistance state of 0.8 kΩ. Note the resistance in (c) is in log-scale and in (d) linear scale.

applying a full reset pulse, followed by multiple set pulses (potentiation). We also point out that we demonstrate the gradual reset with confined PCM cells, but we expect that gradual amorphization will be more efficient in mushroom cells and bridge devices because they are less limited by interfaces and contacts, and therefore have greater dependence on the volume of the amorphous phase compared with confined cells [15].

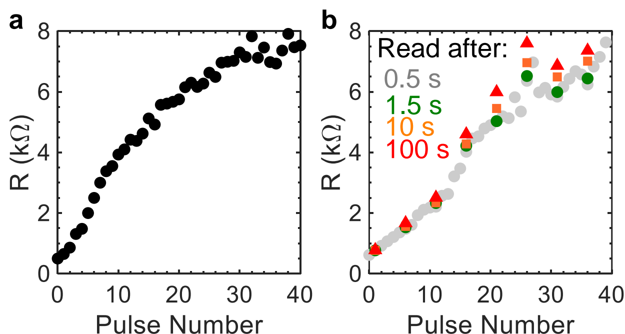

Fig. 4. Resistance drift. (a) Read resistance *vs.* number of pulses showing partial reset measurement without drift test. (b) Resistance drift effect for partial reset. The resistance is read every 5 pulses after 1.5 s, 10 s and 100 s (green circle, orange square and red triangle, respectively).

To better understand the nature of the obtained multilevel states we perform electrical analysis, including threshold voltage characterization, and resistance *vs.* temperature measurements up to the crystallization temperature. We measured the threshold voltage for different intermediate states because it can represent the change in the amorphous volume due to fixed electric field at the threshold point [23], and because the Ovonic threshold switching phenomenon is a unique signature of amorphous chalcogenide semiconductors [24].

Current *vs.* voltage (*I-V*) curves for different states are shown in Fig. 3a. The increasing threshold voltage, from ~0.2 to ~0.8 V illustrates the presence of a mixed crystalline-amorphous phase, with increasing amorphous volume corresponding to higher resistance. In addition, the temperature-dependent resistance of intermediates states (Fig. 3b-d) show an increase in the (negative) temperature coefficient of resistance (TCR) at higher resistance states, and a drop in the resistance at the crystallization temperature to the fcc phase (~450 K) indicating presence of partial amorphization rather than mixed fcc-hexagonal phase.

Finally, we explore the effect of resistance drift on our sub-ns analog reset scheme. This is an important phenomenon to investigate because it can severely limit the accuracy of conductance tuning, depending on the timescale of the training. In this test, we perform read operations after five programming pulses in time steps of 1.5 s, 10 s, and 100 s (see Fig. 4). Drift becomes more prominent at higher resistance states, as expected, owing to larger volume of amorphous phase [21–24].

Interestingly, the drift effect is "erased" by the subsequent reset pulses. This is shown in Fig. 4b, where the resistance state after a drift measurement (color markers in Fig. 4b) continues from the previous non-drifted state (gray) rather than the "drifted state" (red marker). It should also be noted that a critical conduction path in the PCM must melt to achieve re-amorphization, because heating the material to its melting temperature requires high current and low (transient) resistance. We therefore attribute the gradual change in amorphous volume with increasing number of pulses to the dependence of the melted volume on the initial electrical and thermal resistance of the PCM cell. At constant pulse amplitude, the pulse width must be sufficiently short to allow for such fine control of the obtained amorphous volume and the resulting electrical and thermal resistance. Future work should focus on bi-directional weight update (including potentiation) and improving the precision.

IV. Conclusion

We used sub-nanosecond pulse-width programming scheme to demonstrate analog type reset in PCM. This unique behavior, which is essential for neuromorphic applications, is enabled by pulses shorter than the thermal time constant of a critical PCM volume (here ~1-3 ns). The presented method and results can advance the implementation of PCM technology for future neuromorphic applications, and can help enable training with PCM-based artificial intelligence (AI) hardware.

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