ASIC² ARCHITECTURES SYSTEMS INTELLIGENT COMPUTING INTEGRATED CIRCUITS

Developing an Efficient Synthesis and Mapping Method for 3D RRAM Crossbar Array

Background:

Computing-in-memory (CiM) has been a potential solution to break the memory wall and energy wall brought by the conventional computer architecture that separates the computing units and memory units. RRAM-based stateful logic is a kind of CiM that could implement any function in RRAM crossbar array. There are some efficient synthesis and mapping methods for 2D RRAM crossbar array. 3D RRAM crossbar array is denser and can support stateful logic in adjacent layers. The added dimension has created the flexibility to place the stateful logic in 3 dimensions instead of only 2 dimensions. However, there is few synthesis and mapping methods that could efficiently take advantage of the 3-dimension flexibility.

Project:

In this project, we develop a new synthesis and mapping method the RRAM-based stateful logic by taking use of the architecture of 3D RRAM crossbar array. The proposed method would be compared with the method of naively extending the conventional synthesis and mapping method for 2D crossbar to 3D in terms of cell usage, latency, and endurance.

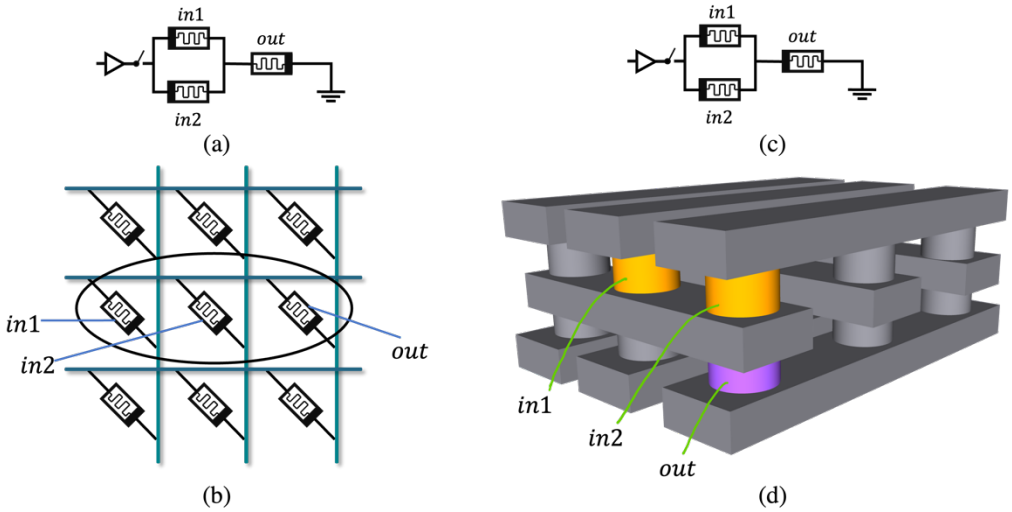

Figure: (a) A NOR logic made by 3 cells (*out* is **parallel** with *in1* and *in2*); (b) A NOR logic in a 2D crossbar array; (c) A NOR logic made by 3 cells (*out* is **antiparallel** with *in1* and *in2*); (d) A NOR logic in a 3D crossbar array

Prerequisites:

- **Courses:** Advanced Circuits and Architectures with Memristors or Introduction to VLSI
- **Skill:** python

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