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Harnessing Conductive Oxide Interfaces for Resistive Random-Access Memories

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Two-dimensional electron gases (2DEGs) can be formed at some oxide interfaces, providing a fertile ground for creating extraordinary physical properties. These properties can be exploited in various novel electronic devices such as transistors, gas sensors, and spintronic devices. Recently several works have demonstrated the application of 2DEGs for resistive random-access memories (RRAMs). We briefly review the basics of oxide 2DEGs, emphasizing scalability and maturity and describing a recent trend of progression from epitaxial oxide interfaces (such as $LaAlO_3/SrTiO_3$) to simple and highly scalable amorphous-polycrystalline systems (e.g., Al_2O_3/TiO_2). We critically describe and compare recent RRAM devices based on these systems and highlight the possible advantages and potential of 2DEGs systems for RRAM applications. We consider the immediate challenges to revolve around scaling from one device to large arrays, where further progress with series resistance reduction and fabrication techniques needs to be made. We conclude by laying out some of the opportunities presented by 2DEGs based RRAM, including increased tunability and design flexibility, which could, in turn, provide advantages for multi-level capabilities.

Keywords: oxide interfaces, resistive random-access memories, device physics, oxide electronics, oxide electronic devices

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INTRODUCTION

Two-dimensional electron gases (2DEGs) can be formed at some oxides interfaces [1]. These oxide interfaces provided a fertile ground for the discovery and manipulation of extraordinary physics, such as superconductivity [2–5], magnetism [6, 7], magnetoelectric coupling [8, 9], Rashba spin-orbit coupling [10], persistent photoconductivity [11, 12], and integer/fractional quantum Hall effect [13, 14]. Over the last decade, leveraging these phenomena towards various devices, such as transistors [15–19], diodes [20], gas sensors [21], spintronic devices [22, 23], and memory devices [24–29], has drawn considerable attention. In addition to the exotic phenomena listed above, the emergence of a high sheet density of electrons (typically 10^{12}~10^{15} cm^{-2}) between two insulators is already attractive for some devices, such as in the role of channels or back electrodes. We note that for the sake of convenience and simplicity, we very broadly use the term 2DEGs as a general name for conductive oxide interfaces, covering 2D, quasi-2D systems, and conducting interfaces where the dimensionality is not well-defined.

Oxide 2DEGs were first reported in epitaxial oxide interfaces, where a complex oxide such as $LaAlO_3$ is grown, typically by pulsed laser deposition (PLD), on a single-crystal oxide substrate, typically $SrTiO_3$ [1, 2] (**Figure 1A**). Therefore, forming such 2DEGs requires epitaxial oxide thin film deposition at high temperatures. Exploiting 2DEGs for novel electronic devices will significantly

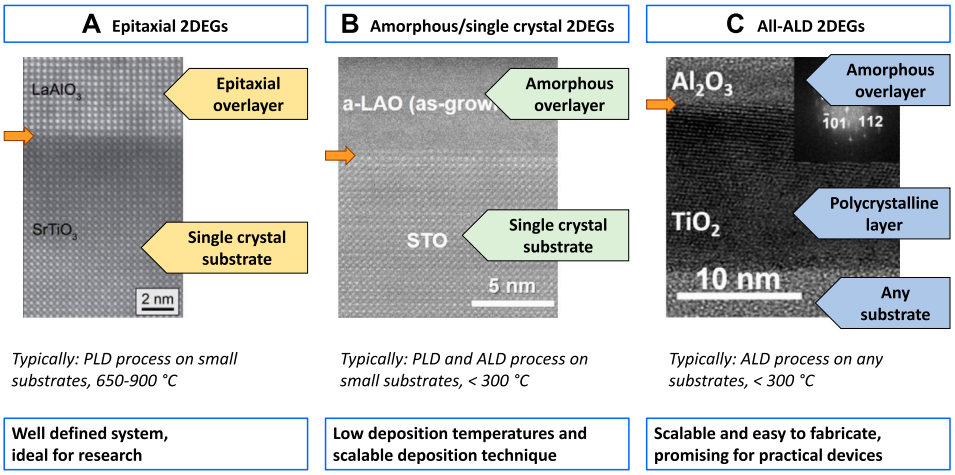

FIGURE 1 | Three different 2DEGs material systems at oxide interfaces of **(A)** Epitaxial 2DEGs [2], **(B)** amorphous oxide on single crystal oxide substrates [62], and **(C)** All-ALD 2DEGs [32]. The orange arrows indicate the position of the conductive oxide interfaces.

benefit from simplifying the materials and deposition methods, where low-temperature, scalable, and microelectronics-compatible approaches are of considerable advantage. Later work has demonstrated that 2DEGs can be formed at more simple interfaces, between amorphous and single-crystalline oxides [30, 31] with the benefit of room temperature preparation. Recently 2DEGs were shown to form even at amorphous/polycrystalline oxide interfaces [17, 21, 32, 33] (**Figure 1C**). Furthermore, the oxide deposition temperatures were reduced from 650-900°C to 25–300°C, and the deposition techniques have been extended from PLD to the more scalable atomic layer deposition (ALD), which is widely used by the microelectronics industry.

Among their various device prospects, recently, 2DEGs were utilized for resistive random-access memories (RRAMs) [24–28]. RRAM devices [34–36] are highly attractive for the next-generation memories [37, 38] and new computing paradigms [39–46]. The potential of 2DEGs in this role has yet to be critically discussed. In this mini review, we briefly review the oxide material systems hosting 2DEGs, focus on their application in the RRAM devices, and finally discuss the challenges and opportunities for 2DEGs in RRAM applications.

Two-Dimensional Electron Gases Formed at Oxide Interfaces

The 2DEG formed in the oxide material system was first observed at the atomically sharp interface between epitaxial $LaAlO_3$ and single-crystalline $SrTiO_3$ substrates, each insulating on its own [1, 2] (**Figure 1A**). In parallel to significant research into the fundamentals of this rich 2D system [47–49], 2DEGs were reported in dozens of other oxide combinations, such as $GdTiO_3/SrTiO_3$ [50] and $NdTiO_3/SrTiO_3$ [51].

The origin of the 2DEG formed at the $LaAlO_3/SrTiO_3$ interface was initially ascribed to polar discontinuity, commonly referred to as the "polar catastrophe". The $LaAlO_3$ film consisting of charge-alternating planes of LaO^+ and AlO_2^- [52] is grown epitaxially on a TiO_2-terminated $SrTiO_3$ substrate. An electrostatic potential builds up in the $LaAlO_3$ layer and increases with its thickness. As the thickness of the $LaAlO_3$ film increases to four unit cells or higher, the voltage drop becomes sufficiently large for electrons to move from the surface of the $LaAlO_3$ film to the $LaAlO_3/SrTiO_3$ interface, where they occupy delocalized Ti 3d states in $SrTiO_3$ [52–56].

Besides the polar catastrophe mechanism, the ionic aspect of the interface plays an important role in its electronic properties [57]. Interdiffusion and intermixing of atoms across the interface [58] and oxygen vacancies [59–61] can account for the 2DEG formation via various ionic doping mechanisms. It is further argued that polar effects can drive such ionic mechanisms by making them more energetically favorable [62, 63]. These ionic features of the interface open opportunities to simplify the 2DEG material systems to non-polar, amorphous oxide materials. As such, the formation of 2DEG and their properties are strongly dependent on the material system, deposition method, and post-deposition processes.

The growth of epitaxial oxides requires slow and high-temperature (typically 650–900°C) processes using PLD or molecular-beam epitaxy (MBE). These features, and their low scalability (PLD), make the 2DEGs formed at epitaxial oxide interfaces incompatible with CMOS processes and large-scale fabrication. The use of amorphous oxide on single crystal oxide substrates [16, 24, 30, 31, 64–68] (**Figure 1B**) lowered the oxide deposition temperatures to <300°C and expanded the deposition methods to ALD. The use of amorphous oxides deposited on polycrystalline oxide [17, 21, 25, 32, 33, 69], which we term "All-ALD 2DEGs", provides a great advantage towards scalability and integration with existing and future technologies (**Figure 1C**). We note that significant progress has been demonstrated in MBE-based integration of epitaxial oxide 2DEGs systems with silicon [70–72] and other semiconductors [73, 74]. Still, while potentially scalable

[75], they remain slow, expensive, and high temperature (~600°C) and thus fall far behind the non-epitaxial ALD approaches.

This chronological trend of simplifying the materials and fabrication techniques has seen the transition from epitaxial interfaces (e.g., single crystalline $LaAlO_3$/single crystalline $SrTiO_3$, **Figure 1A**) to amorphous oxides on single-crystals (e.g., a-$LaAlO_3$/single crystalline $SrTiO_3$, **Figure 1B**), and recently to All-ALD 2DEGs with amorphous-polycrystalline systems (e.g., amorphous Al_2O_3/polycrystalline TiO_2, **Figure 1C**). The third system allows deposition temperatures to decrease to <300°C, well below the requirements of CMOS backend processes. Such advances hold the significant promise of realizing the potential of 2DEGs into practical devices and maturing them from single device lab-scale demonstrators towards scalable and microelectronics-compatible technology. In this mini review, we focus on the application of 2DEGs in RRAM devices.

Resistive Random-Access Memory Devices

The RRAM device has a simple metal-insulator-metal (MIM) structure with a resistive switching layer(s) sandwiched between two electrodes. It stores information by using different resistance states. For binary information storage, "0" and "1" information can be stored within one device cell using high and low resistance states (HRS and LRS, respectively). For multi-level information storage, more than a single bit of information can be stored within a single device cell using multiple resistance states. For example, information of "00", "01", "10", and "11" can be stored within one device cell using four different resistance states. Besides information storage, RRAM devices are also promising for new computing paradigms [39–44], which are faster in speed and lower in energy consumption. The resistive switching processes can accompany typical physical/chemical effects such as electrochemical/thermochemical reactions or metal-insulator transitions [34, 36, 40]. In the conductive filament (CF)-type RRAM devices, the mechanism of the resistance switching is the formation and disruption of conductive filaments (nanometric in diameter) within the resistive switching layer (a few nanometers in thickness) under external electrical stimuli. RRAM devices have many attractive features, such as small device area (4 F^2), fast switching speed (<1 ns) [76], high scalability [77–79], 3D integration capability [80, 81], and low energy consumption for resistance switching (<10 pJ/bit) [82, 83]. Based on the type of the conductive filaments, the RRAM devices can be divided into two types, which are the valence change memory (VCM) [76] and the electrochemical metallization memory (ECM) [84–86], which is also known as conductive-bridge RAM (CBRAM).

Two-Dimensional Electron Gases at Oxide Interfaces for Resistive Random-Access Memory Applications

Recently, 2DEGs have been leveraged for forming different types of RRAMs, by replacing one of the metal electrodes. This path can potentially increase design flexibility, enhance performance, and yield additional interesting properties.

In VCM devices, the 2DEG acts as an unconventional bottom electrode. In addition to the (electronic) conductivity of 2DEGs, their inherent ionic defects and instabilities can induce, interact with, and be utilized to control the resistive switching process. The oxide forming the 2DEG adjacent to the top electrode also acts as the resistive switching layer. The oxygen vacancies drift under the external electric field and create defect-induced gap states within the resistive switching layer during the resistive switching process. Whereas the electronic conduction property of 2DEGs performs as the function of a traditional metal bottom electrode. Several VCM RRAM devices have been recently reported, leveraging such 2DEG electrodes. These include Pt/$LaAlO_3$/$SrTiO_3$ [26], indium tin oxide (ITO)/$LaAlO_3$/$SrTiO_3$ [28], Pt/Ta_2O_{5-y}/Ta_2O_{5-x}/$SrTiO_3$ [27], and Pt/Al_2O_3/$SrTiO_3$ [24].

Wu et al. [26] were the first to use oxide 2DEGs in RRAM devices. Their device utilized the 2DEG formed at the epitaxial $LaAlO_3$/$SrTiO_3$ interface as the bottom electrode, the $LaAlO_3$ layer as the resistive switching layer, and the Pt layer as the top electrode layer. The conduction mechanisms are Ohmic transport at the low resistance state (LRS) and tunneling at the high resistance state (HRS). The $LaAlO_3$ layer was deposited on TiO_2-terminated $SrTiO_3$ (001) substrates using PLD at 800°C. The device switches based on the electric-field-induced drift of positively charged oxygen vacancies across the $LaAlO_3$/$SrTiO_3$ interface and the creation of defect-induced gap states within the ultrathin $LaAlO_3$ layer. Wu et al. [28] further substituted the Pt top electrode with ITO and demonstrated an optically transparent RRAM device. After replacing the Pt with ITO, the resistance window remained at 100. In contrast, the overall resistance level increased by five orders of magnitude from HRS at 10^4 Ω and LRS at 10^2 Ω to HRS at 10^9 and LRS at 10^7 Ω. The Pt/$LaAlO_3$/$SrTiO_3$ and ITO/$LaAlO_3$/$SrTiO_3$ structured devices both showed 2000 cycle endurance and 12 h retention, comparable to those in the Pt/$LaAlO_3$/Nb:$SrTiO_3$ structured devices [87].

Joung et al. [27] reported amorphous TaO_x/single crystal $SrTiO_3$ based VCM. Ta_2O_{5-y} (TO2)/Ta_2O_{5-x} (TO1) bilayer of TaO_x was deposited using PLD at 200°C under 70–100 mTorr oxygen (TO2) and at 700°C under 0.5 mTorr oxygen (TO1). The interface conductivity results from ionic defects formed during the high-temperature step and possibly kinetic damage from the PLD process. This use of amorphous layers constitutes progress toward simplifying the materials and deposition techniques. However, the PLD process's high temperature and low scalability remain incompatible with practical applications. The devices showed 2000 cycles endurance and 10^5 s retention. The best endurance and retention of TaO_x based RRAM devices are reported in Pt/$Ta_2O_{5-\delta}$/$TaO_{2-\beta}$/Pt structured devices [88] with 10^9 endurance cycles and 7.2×10^6 s retention.

Miron et al. [24] continued this trend of using amorphous layers for the 2DEG formation but focused on simple, low temperature, and scalable deposition. They reported amorphous Al_2O_3/single crystal $SrTiO_3$ based VCM devices, where the Al_2O_3 layer was deposited using ALD, with a low deposition temperature of 300°C (**Figure 2A**). The devices showed a large OFF/ON resistance ratio of ~10^6 and low operation currents down to 10^{-13} A (HRS,

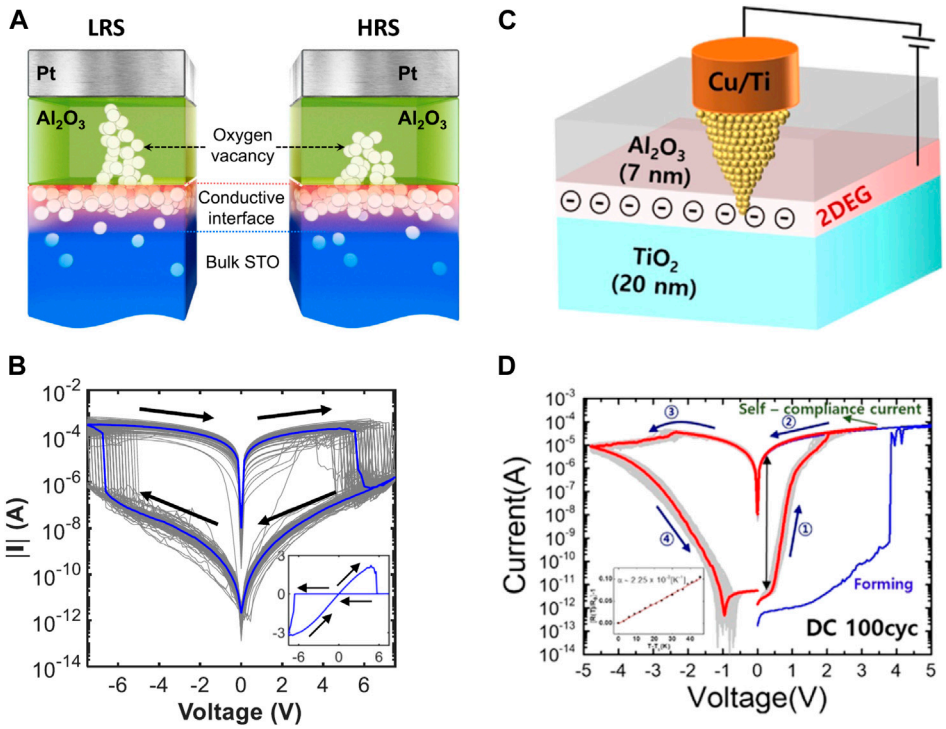

FIGURE 2 | Recent examples of 2DEGs-based RRAM devices. **(A)** Schematic of a VCM-type RRAM device based on 2DEGs formed between amorphous ALD-Al_2O_3 and single-crystalline $SrTiO_3$ (STO) [24]. **(C)** Schematic of a CBRAM-type RRAM device based on the scalable All-ALD 2DEGs [25]. Panels **(B)** and **(D)** both present 100 cycles of consecutive DC current-voltage sweeps of the VCM and CBRAM devices (respectively).

Figure 2B) with good cycle-to-cycle uniformity. The memory is based on the formation and rupture of oxygen vacancies filaments inside the Al_2O_3 layer. The oxygen vacancies driven from the interface into the insulating oxide under high electric fields are the key in enabling the resistive switching behavior. A key feature of this work is the application of low-defect Al_2O_3 [89], where the 2DEG serves as the bottom electrode and as the source of oxygen vacancies. The oxygen vacancies are injected by the electric field into the insulating Al_2O_3 to form the conductive filament. The practical consequence of this approach is the trigger of resistive switching behavior as compared to the $Pt/Al_2O_3/Nb:SrTiO_3$ stuctured device [89] and a large OFF/ON resistance ratio afforded by using a good insulator of Al_2O_3 as the resistive switching layer and the 2DEG as the bottom electrode [24, 90, 91]. The key shortcoming here was the large set/reset voltages, on the order of ±7 V, another consequence of the insulating Al_2O_3. Further optimization of these devices, focusing on the insulator thickness, is expected to yield a better tradeoff between lowering the set/reset voltages while preserving the high OFF/ON resistance ratios.

As discussed earlier, All-ALD 2DEGs provide the most practical and scalable approach for 2DEG formation. Kim et al. [25] reported the first RRAM application of such 2DEGs, the only reported 2DEG CBRAM device (**Figures 2C,D**). They demonstrated a Cu conductive filament device based on 2DEG formed between amorphous Al_2O_3 and polycrystalline anatase TiO_2 (**Figure 1C**). Both materials were fabricated by ALD (250°C) and, most importantly, without a crystalline substrate. The devices showed good endurance of 10^7 cycles and a high OFF/ON resistance ratio of 10^6. Four different HRS levels are also achieved by adjusting the amplitude of the operation voltage pulses. The LRS kept constant, whereas the HRS increased as the device areas decreased. This resistance and device area dependency is beneficial for device area scaling. A higher OFF/ON resistance ratio and a lower current level can be achieved as the device area becomes smaller. The Cu conductive filament formed at LRS, observed by TEM, is about 20 nm in diameter. A device diameter of 20 nm is, in principle, the area scaling limit of such a device. This device also showed better endurance and retention behavior than $Cu/Al_2O_3/Pt$ structured devices [93, 94]. We highlight again the significant progress made by circumventing a single crystalline substrate, which allows integrating these devices on many substrates, such as the backend of silicon chips, flexible electronics [21], and others.

In more conventional VCM-type RRAM devices, the resistive-switching material typically contains some initial number of defects rearranged during the first forming process. A difference of 2DEGs-based VCM RRAM is that one can start with a fairly insulating material and use the 2DEG as *an extrinsic source of defects* [24]. This provides 2DEGs-based VCM RRAM with significantly larger OFF/ON resistance ratios compared to more conventional approaches. The high OFF/ON resistance ratio offers potential for multi-level resistance operation. The

TABLE 1 | Comparison of device performances.

Device Structure	Device Size	Forming (Yes/No, $V_{forming}$, Icc)	Top electrode	Resistive switching layer	Bottom electrode	Switching polarity	SET/ RESET Voltage (DC)	Max Iset/I_{CC} (DC)	Max Ireset (DC)	SET/RESET Voltage (AC)	SET/ RESET Switching speed (AC)	HRS/ LRS (Ω)	Resistance ratio	Endurance (cycles)	Retention (s)
Pt/$LaAlO_3$/ $SrTiO_3$ [26]	2.25 × 10^4 μm^2	Yes, -4 V, 30 mA	Pt	$LaAlO_3$	$LaAlO_3$/ $SrTiO_3$ 2DEG	bipolar	−4 V/+4 V	30 mA/No I_{CC}	30 mA	−4 V/+4 V −4 V/+9 V	5 ns/100 μs 5 ns/1 μs	10^4/10^2	10^2	2000	>4.32 × 10^3 (@25°C)
ITO/ $LaAlO_3$/ $SrTiO_3$ [28]	9 × 10^4 μm^2	Yes, -3.3 V, 30 μA	ITO	$LaAlO_3$	$LaAlO_3$/ $SrTiO_3$ 2DEG	bipolar	−1.5 V/+5 V	30 μA/No I_{CC}	0.5 nA	−5 V/+5 V	Not given	10^9/10^7	10^2	2000	>4 × 10^4 (@25°C)
Pt/$LaAlO_3$/ Nb: $SrTiO_3$ [87]	10^6 to 10^4 μm^2	Yes, -13 V to -40 V (P_{O2} and t_{ox} dependent), I_{CC} not given	Pt	$LaAlO_3$	Nb: $SrTiO_3$	bipolar	−6 V/+6 V	70 mA/no I_{CC}	10 mA	−8 V/+8 V	Not given	10^6/10^3	10^3	2000	>4.32 × 10^3 (@25°C)
ITO/ $LaAlO_3$/ ITO [94]	1.13 × 10^6 μm^2 (⌀ = 1,200 μm)	Yes, -1 V to -2.6 V (P_{O2} dependent), 10 mA	ITO	$LaAlO_3$	ITO	bipolar	Not given/+3 V	Not given	5–10 mA	Not given	Not given	10^3/10^2	10	100	Not given
Pt/Ta_2O_{5-y}/ Ta_2O_{5-x}/ STO [27]	490.63 μm^2 (⌀ = 25 μm)	Not mentioned	Pt	Ta_2O_{5-y}	Ta_2O_{5-x}/ STO 2DEG	bipolar	+4 V/−2.5 V	2 μA/no I_{CC}	1 μA	Not given	Not given	10^{12}/ 10^8	10^4	2,900	>10^5 (@25°C)
Pt/$Ta_2O_{5-\delta}$/$TaO_{2-\beta}$/Pt [88]	0.25 μm^2	Not mentioned	Pt	$Ta_2O_{5-\delta}$/$TaO_{2-\beta}$	Pt	bipolar	−0.9 V/+2 V	170 μA/ 170 μA	170 μA	2 V/−1.5 V	10 ns	10^3/10^2	10	10^9	1.08 × 10^7 (@150°C)
Pt/Al_2O_3/ STO [24]	2.7 × 10^4 to 1.5 × 10^5 μm^2	Yes, -6 V to −4 V, 0.1 mA	Pt	Al_2O_3	Al_2O_3/STO 2DEG	bipolar	−7 V/+7 V	0.5 mA/not mentioned	0.5 mA	Not given	Not given	10^{10}/ 10^4	10^6	100	Not Given
Pt/Al_2O_3/ Nb: $SrTiO_3$ [89]	No resistive switching behavior														
Pt/Al_2O_3/ TiN [90]	2.5 × 10^{-3} μm^2	Yes, 7 V, <10 μA, no I_{CC}	Pt	Al_2O_3	TiN	Bipolar	+3 V/−2 V	<300 μA/ 300 μA	<1 mA	8 V/−4 V	10 ns/10 ns	10^6/10^3	10^3	1,000	Not given
Ni/Al_2O_3/ Pt [90]	10^4 μm^2	Yes, 5 V, 500 μA	Ni	Al_2O_3	Pt	Bipolar	+1.2 V/ −0.45 V to −0.6 V	500 μA/ 500 μA	<2 mA	1.5 V/−0.4 V to −0.58 V	5 ms/5 ms	2.8 × 10^3 to 2.2 × 10^3/470	6 to 4.7	100	10_3 s
Cu/Al_2O_3/ TiO_2 [25]	0.02–340 μm^2	Yes, 1 to 5V, no Icc (self-compliance), I_{max}<0.1 mA	Cu	Al_2O_3	Al_2O_3/TiO_2 2DEG	bipolar	+3 V/−5 V	<0.1 mA/no I_{CC} (self-compliance)	<0.1 mA	Not given	500–800 ns	10^{11}/ 10^5	10^6	10^7	10^6 (@85°C)
Cu/Al_2O_3/ Pt [92]	3.14 × 10^4 μm^2 (⌀ = 200 μm)	Yes, 8 V, 200 μA	Cu	Al_2O_3	Pt	bipolar	0.3–1.2 V/-0.1 V to −0.7 V	150 μA/ 150 μA	<0.1 mA	Not given	Not given	10^9/10^3	10^6	2000	10^5
Cu/Ti/ Al_2O_3/ Pt [93]	0.05 μm^2 (via hole ⌀ = 0.25 μm)	Yes, 1.1 V, 200 μA	Cu/Ti	Al_2O_3	Pt	bipolar	0.3–0.7 V/ −0.1 V to −0.3 V	200 μA/ 200 μA	~0.1 mA	Not given	Not given	10^9/10^4	10^5	Not given	10^4
Pt/WO_x/ W [96]	2 × 10^{-3} μm^2	No, Forming free	Pt	WO_x	W	bipolar	1 V/−1 V	4 mA/no I_{CC}	<0.2 mA	+1.25 V/-1 V	5 μs/5 μs	10^6/10^4	10^2	10^7	Not Given
IrO_x/Al_2O_3/ TiO_x/ TiN [97]	0.24 μm^2	Yes, 7.5–20 V, 100 μA	IrO_x	Al_2O_3 (2–8 nm)/ TiO_x	TiN	bipolar	3.5–5.4 V/ −3 V	100 μA/ 100 μA	<15 μA	+3 V–5.5 V/-3 V	500 μs/ 10 ms	4 × 10^6 to 10^7/ 0.4 × 10^6 to	10.8 to 21.62	10^5 to 10^6	Not Given

(Continued on following page)

TABLE 1 | (*Continued*) Comparison of device performances.

Device Structure	Device Size	Forming (Yes/No, $V_{forming}$, Icc)	Top electrode	Resistive switching layer	Bottom electrode	Switching polarity	SET/ RESET Voltage (DC)	Max Iset/I_{CC} (DC)	Max Ireset (DC)	SET/RESET Voltage (AC)	SET/ RESET Switching speed (AC)	HRS/ LRS (Ω)	Resistance ratio	Endurance (cycles)	Retention (s)
TiN/Ti/TiO_{2-x}/TiO_{2-y}/ Au [98]	10^4 μm^2	No, Forming free	TiN/Ti	TiO_{2-x}/ TiO_{2-y}	Au	bipolar	3 V/−3 V	<0.1 mA/No I_{CC} (self-compliance)	<0.1 μA	+8 V/−8 V	10 ms/ 10 ms	1.2×10^6 to 4×10^8	2 to 3.6×10^3	Not Given	Not Given
Ru/TiO_{2-x}/ HfO_x/ Ru [99]	10^4 μm^2	Yes, 4–4.5 V, 5 mA	Ru	TiO_{2-x}/HfO_2	Ru	bipolar	2 V/−1.5 V	5 mA/5 mA	<5 mA	Not given	Not given	10^3/10^2	10	10^4	10^5
Ni/GeO/ $SrTiO_3$/ TaN [100]	11304 μm^2	Not given	Ni	GeO/$SrTiO_3$	TaN	bipolar	−0.3 V to −1.2 V/ 0.13–0.3 V	3.5 μA/No I_{CC} (self-compliance)	0.12 nA	−1.5 V/0.5 V	50 ns/50 ns	10^{12}/ 10^6	10^6	10^6	4×10^5 (@85°C)

broader ratio provides more room for improvement of this feature, as more distinct states can fit this wider resistivity range [94]. However, multi-level behavior has yet to be reported in 2DEGs based VCM devices due to the abruptness of their switching. Another consequence of the high OFF/ON resistance ratio is extremely low current at HRS, which benefits low-power operation. A comparison of 2DEG based RRAM devices, devices that show close similarity to the 2DEG based device structures, and some other RRAM devices are listed in **Table 1**.

We consider the progress made with the All-ALD 2DEGs [25, 33] to be a defining point. The All-ALD 2DEGs have liberated 2DEGs from small and expensive single-crystal substrates and from costly high-temperature fabrication processes. 2DEGs are now being fabricated by ALD on many substrates while keeping a low thermal budget and using low-cost, highly scalable, mature, and microelectronics-compatible techniques. The use of anatase TiO_2 provides another advantage of a potentially more conductive 2DEG compared to the $LaAlO_3/SrTiO_3$ interface at room temperature [64] and offers tunability of the conductivity [32, 33]. Higher conductivity of the 2DEG is desirable in RRAM applications because the resistance of the bottom electrode is in series with the resistive switching layer, making lower resistance beneficial for stabilizing the resistive switching behavior, and for reducing the operating power. These issues become more important when considering integrating devices into a crossbar structure.

CHALLENGES

The 2DEGs based RRAM devices reported so far are all single device demonstrations. Integration of the 2DEGs based RRAM devices into a crossbar array or 3D vertical structures poses an open challenge, which requires several issues to be addressed. Due to their high series resistance, the relatively high sheet resistance of many 2DEGs (typically $>10^4\ \Omega/\square$) makes it challenging to utilize 2DEGs as thin line bottom electrodes. Beyond increasing the operating voltage (and power), this series resistance of the bottom electrode could further cause a significant spatial distribution of operation voltages across a crossbar array. As such, it remains an important task to reduce the 2DEG resistivity and design new device structures for high-density RRAM integration. Another facet of these challenges is microfabrication: 2DEGs, particularly those driven by defects, can be challenging to pattern efficiently [101–103]. Robust fabrication techniques need to be designed to produce the small features necessary for high-density RRAM arrays. In addition, further flexibility in the tuning of the 2DEG resistivity would provide an advantage for device and array optimization, which would further benefit from a deeper understanding of the 2DEGs-based RRAM switching mechanisms.

OPPORTUNITIES

As discussed earlier, 2DEGs-based RRAMs can feature large, potentially tunable OFF/ON resistance ratios. These provide

prospects of low power operation, allow additional "room" for efficient multi-level resistance states, and provide additional design flexibility and tunability compared to some of the current devices. The 2DEGs-based VCM devices so far all showed abrupt switching processes, resulting in binary resistance states. Further development of these devices into multi-level capabilities will provide considerable functionality benefits. Since 2DEGs are successfully applied as the channel of transistors [15, 16, 19, 32]. This opens routes for integrating both the memory and the peripheral circuits within the same material system and even within the same lithography process steps. This is also a very attractive feature for RRAM devices in crossbar arrays since the crossbar structured RRAM devices require selectors to select different rows and columns.

AUTHOR CONTRIBUTIONS

All authors discussed and designed the structure and scope of the mini-review, which was written by YL. All authors read and commented on the text.

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REFERENCES

1. Ohtomo A, and Hwang HY. A High-Mobility Electron Gas at the $LaAlO_3$/$SrTiO_3$ Heterointerface. *Nature* (2004) 427:423–6. doi:10.1038/nature02308
2. Reyren N, Thiel S, Caviglia AD, Kourkoutis LF, Hammerl G, Richter C, et al. Superconducting Interfaces between Insulating Oxides. *Science* (2007) 317: 1196–9. doi:10.1126/science.1146006
3. Gariglio S, Reyren N, Caviglia AD, and Triscone J-M. Superconductivity at the $LaAlO_3$/$SrTiO_3$ interface. *J Phys Condens Matter* (2009) 21:164213–2. doi:10.1088/0953-8984/21/16/164213
4. Han Y-L, Shen S-C, You J, Li H-O, Luo Z-Z, Li C-J, et al. Two-dimensional Superconductivity at (110) $LaAlO_3$/$SrTiO_3$ Interfaces. *Appl Phys Lett* (2014) 105:192603–8. doi:10.1063/1.4901940
5. Monteiro AMRVL, Groenendijk DJ, Groen I, De Bruijckere J, Gaudenzi R, Van Der Zant HSJ, et al. Two-dimensional Superconductivity at the (111) $LaAlO_3$/$SrTiO_3$ Interface. *Phys Rev B* (2017) 96:1–4. doi:10.1103/PhysRevB.96.020504
6. Brinkman A, Huijben M, Van Zalk M, Huijben J, Zeitler U, Maan JC, et al. Magnetic Effects at the Interface between Non-magnetic Oxides. *Nat Mater* (2007) 6:493–6. doi:10.1038/nmat1931
7. Bert JA, Kalisky B, Bell C, Kim M, Hikita Y, Hwang HY, et al. Direct Imaging of the Coexistence of Ferromagnetism and Superconductivity at the $LaAlO_3$/$SrTiO_3$ Interface. *Nat Phys* (2011) 7:767–71. doi:10.1038/nphys2079
8. Wei L-y., Lian C, and Meng S. Prediction of Two-Dimensional Electron Gas Mediated Magnetoelectric Coupling at Ferroelectric $PbTiO_3$/$SrTiO_3$ Heterostructures. *Phys Rev B* (2017) 95:3–8. doi:10.1103/PhysRevB.95.184102
9. Sun W, Wang W, Chen D, Cheng Z, Jia T, and Wang Y. Giant Magnetoelectric Coupling and Two-Dimensional Electron Gas Regulated by Polarization in $BiFeO_3$/$LaFeO_3$ Heterostructures. *J Phys Chem C* (2019) 123:16393–9. doi:10.1021/acs.jpcc.9b04499
10. Liang H, Cheng L, Wei L, Luo Z, Yu G, Zeng C, et al. Nonmonotonically Tunable Rashba Spin-Orbit Coupling by Multiple-Band Filling Control in $SrTiO_3$-Based Interfaciald-Electron Gases. *Phys Rev B* (2015) 92:1–7. doi:10.1103/PhysRevB.92.075309
11. Tebano A, Fabbri E, Pergolesi D, Balestrino G, and Traversa E. Room-Temperature Giant Persistent Photoconductivity in $SrTiO_3$/$LaAlO_3$ Heterostructures. *ACS Nano* (2012) 6:1278–83. doi:10.1021/nn203991q
12. Tarun MC, Selim FA, and McCluskey MD. Persistent Photoconductivity in Strontium Titanate. *Phys Rev Lett* (2013) 111:1–5. doi:10.1103/PhysRevLett.111.187403
13. Tsukazaki A, Ohtomo A, Kita T, Ohno Y, Ohno H, and Kawasaki M. Quantum Hall Effect in Polar Oxide Heterostructures. *Science* (2007) 315: 1388–91. doi:10.1126/science.1137430
14. Tsukazaki A, Akasaka S, Nakahara K, Ohno Y, Ohno H, Maryenko D, et al. Observation of the Fractional Quantum Hall Effect in an Oxide. *Nat Mater* (2010) 9:889–93. doi:10.1038/nmat2874
15. Kornblum L. Conductive Oxide Interfaces for Field Effect Devices. *Adv Mater Inter* (2019) 6:1900480. doi:10.1002/admi.201900480
16. Moon T, Lee HJ, Hyun SD, Kim BS, Kim HH, and Hwang CS. Origin of the Threshold Voltage Shift in a Transistor with a 2D Electron Gas Channel at the Al_2O_3/$SrTiO_3$ Interface. *Adv Electron Mater* (2020) 6:1901286–8. doi:10.1002/aelm.201901286
17. Lee HJ, Moon T, Hyun SD, Kang S, and Hwang CS. Characterization of a 2D Electron Gas at the Interface of Atomic-Layer Deposited Al_2O_3/ZnO Thin Films for a Field-Effect Transistor. *Adv Electron Mater* (2021) 7:2000876–8. doi:10.1002/aelm.202000876
18. Jany R, Richter C, Woltmann C, Pfanzelt G, Förg B, Rommel M, et al. Monolithically Integrated Circuits from Functional Oxides. *Adv Mater Inter* (2014) 1:1300031. doi:10.1002/admi.201300031
19. Förg B, Richter C, and Mannhart J. Field-effect Devices Utilizing $LaAlO_3$-$SrTiO_3$ Interfaces. *Appl Phys Lett* (2012) 100:053506. doi:10.1063/1.3682102
20. Moon T, Jung HJ, Kim YJ, Park MH, Kim HJ, Kim KD, et al. Research Update: Diode Performance of the Pt/Al_2O_3/two-Dimensional Electron gas/$SrTiO_3$ Structure and its Time-dependent Resistance Evolution. *APL Mater* (2017) 5:042301. doi:10.1063/1.4967280
21. Kim SM, Kim HJ, Jung HJ, Park JY, Seok TJ, Choa YH, et al. High-Performance, Transparent Thin Film Hydrogen Gas Sensor Using 2D Electron Gas at Interface of Oxide Thin Film Heterostructure Grown by Atomic Layer Deposition. *Adv Funct Mater* (2019) 29:1807760. doi:10.1002/adfm.201807760
22. Noël P, Trier F, Vicente Arche LM, Bréhin J, Vaz DC, Garcia V, et al. Non-volatile Electric Control of Spin-Charge Conversion in a $SrTiO_3$ Rashba System. *Nature* (2020) 580:483–6. doi:10.1038/s41586-020-2197-9
23. Varignon J, Vila L, Barthélémy A, and Bibes M. A New Spin for Oxide Interfaces. *Nat Phys* (2018) 14:322–5. doi:10.1038/s41567-018-0112-1
24. Miron D, Cohen-Azarzar D, Hoffer B, Baskin M, Kvatinsky S, Yalon E, et al. Oxide 2D Electron Gases as a Reservoir of Defects for Resistive Switching. *Appl Phys Lett* (2020) 116:223503. doi:10.1063/5.0003590
25. Kim SM, Kim HJ, Jung HJ, Kim SH, Park J-Y, Seok TJ, et al. Highly Uniform Resistive Switching Performances Using Two-Dimensional Electron Gas at a Thin-Film Heterostructure for Conductive Bridge Random Access Memory. *ACS Appl Mater Inter* (2019) 11:30028–36. doi:10.1021/acsami.9b08941
26. Wu S, Luo X, Turner S, Peng H, Lin W, Ding J, et al. Nonvolatile Resistive Switching in Pt/$LaAlO_3$/$SrTiO_3$ Heterostructures. *Phys Rev X* (2013) 3: 041027. doi:10.1103/PhysRevX.3.041027
27. Joung JG, Kim S-I, Moon SY, Kim D-H, Gwon HJ, Hong S-H, et al. Nonvolatile Resistance Switching on Two-Dimensional Electron Gas. *ACS Appl Mater Inter* (2014) 6:17785–91. doi:10.1021/am504354c
28. Wu S, Ren L, Qing J, Yu F, Yang K, Yang M, et al. Bipolar Resistance Switching in Transparent ITO/$LaAlO_3$/$SrTiO_3$ Memristors. *ACS Appl Mater Inter* (2014) 6:8575–9. doi:10.1021/am501387w
29. Gao Z, Huang X, Li P, Wang L, Wei L, Zhang W, et al. Reversible Resistance Switching of 2D Electron Gas at $LaAlO_3$/$SrTiO_3$ Heterointerface. *Adv Mater Inter* (2018) 5:1701565–8. doi:10.1002/admi.201701565

30. Chen Y, Pryds N, Kleibeuker JE, Koster G, Sun J, Stamate E, et al. Metallic and Insulating Interfaces of Amorphous $SrTiO_3$-Based Oxide Heterostructures. *Nano Lett* (2011) 11:3774–8. doi:10.1021/nl201821j
31. Moon SY, Moon CW, Chang HJ, Kim T, Kang C-Y, Choi H-J, et al. Thermal Stability of 2DEG at Amorphous $LaAlO_3$/crystalline $SrTiO_3$ Heterointerfaces. *Nano Convergence* (2016) 3:1–6. doi:10.1186/s40580-016-0067-9
32. Seok TJ, Liu Y, Jung HJ, Kim SB, Kim DH, Kim SM, et al. Field-Effect Device Using Quasi-Two-Dimensional Electron Gas in Mass-Producible Atomic-Layer-Deposited Al_2O_3/TiO_2 Ultrathin (<10 Nm) Film Heterostructures. *ACS Nano* (2018) 12:10403–9. doi:10.1021/acsnano.8b05891
33. Seok TJ, Liu Y, Choi JH, Kim HJ, Kim DH, Kim SM, et al. *In Situ* Observation of Two-Dimensional Electron Gas Creation at the Interface of an Atomic Layer-Deposited Al_2O_3/TiO_2 Thin-Film Heterostructure. *Chem Mater* (2020) 32:7662–9. doi:10.1021/acs.chemmater.0c01572
34. Waser R, Dittmann R, Staikov G, Szot K, Staikov C, and Szot K. Redox-Based Resistive Switching Memories - Nanoionic Mechanisms, Prospects, and Challenges. *Adv Mater* (2009) 21:2632–63. doi:10.1002/adma.200900375
35. Yang JJ, Strukov DB, and Stewart DR. Memristive Devices for Computing. *Nat Nanotech* (2013) 8:13–24. doi:10.1038/nnano.2012.240
36. Wong H-SP, Lee H-Y, Yu S, Chen Y-S, Wu Y, Chen P-S, et al. Metal-oxide RRAM. *Proc IEEE* (2012) 100:1951–70. doi:10.1109/JPROC.2012.2190369
37. Lee SR, Kim Y-B, Chang M, Kim KM, Lee CB, Hur JH, Park G-S, Lee D, Lee M-J, Kim CJ, et al. Multi-level Switching of Triple-Layered TaO_x RRAM with Excellent Reliability for Storage Class Memory In: Symposium on VLSI Technology (VLSIT). Honolulu, HI, USA: IEEE (2012) p. 71–2. doi:10.1109/VLSIT.2012.6242466
38. Hsu C-W, Wang I-T, Lo C-L, Chiang M, Jang W, Lin C-H, and Hou T-H. Self-Rectifying Bipolar TaO_x/TiO_2 RRAM with Superior Endurance over 10^{12} Cycles for 3D High-Density Storage-Class Memory In: Symposium on VLSI Circuits (VLSI). Kyoto, Japan: IEEE (2013). p. T166–T167.
39. Xia Q, and Yang JJ. Memristive Crossbar Arrays for Brain-Inspired Computing. *Nat Mater* (2019) 18:309–23. doi:10.1038/s41563-019-0291-x
40. Dittmann R, and Strachan JP. Redox-based Memristive Devices for New Computing Paradigm. *APL Mater* (2019) 7:110903. doi:10.1063/1.5129101
41. Sun Z, Pedretti G, Ambrosi E, Bricalli A, Wang W, and Ielmini D. Solving Matrix Equations in One Step with Cross-point Resistive Arrays. *Proc Natl Acad Sci USA* (2019) 116:4123–8. doi:10.1073/pnas.1815682116
42. Wang W, Song W, Yao P, Li Y, Van Nostrand J, Qiu Q, et al. Integration and Co-design of Memristive Devices and Algorithms for Artificial Intelligence. *iScience* (2020) 23:101809. doi:10.1016/j.isci.2020.101809
43. Ielmini D, and Ambrogio S. Emerging Neuromorphic Devices. *Nanotechnology* (2020) 31:092001. doi:10.1088/1361-6528/ab554b
44. Zidan MA, Strachan JP, and Lu WD. The Future of Electronics Based on Memristive Systems. *Nat Electron* (2018) 1:22–9. doi:10.1038/s41928-017-0006-8
45. Kvatinsky S, Belousov D, Liman S, Satat G, Wald N, Friedman EG, et al. MAGIC-Memristor-Aided Logic. *IEEE Trans Circuits Syst* (2014) 61:895–9. doi:10.1109/TCSII.2014.2357292
46. Christensen DV, Dittmann R, Linares-Barranco B, Sebastian A, Gallo ML, Redaelli A, et al. Roadmap on Neuromorphic Computing and Engineering, *arXiv Prepr* (2021).
47. Pai Y-Y, Tylan-Tyler A, Irvin P, and Levy J. Physics of $SrTiO_3$-Based Heterostructures and Nanostructures: a Review. *Rep Prog Phys* (2018) 81:036503. doi:10.1088/1361-6633/aa892d
48. Liu Z, Annadi A, and Ariando. Two-Dimensional Electron Gas at $LaAlO_3$/$SrTiO_3$ Interfaces. In: J Yi and S Li, editors. *Functional Materials and Electronics*. Apple Academic Press (2018) p. 35–95. doi:10.1201/9781315167367
49. Pryds N, and Esposito V. When Two Become One: An Insight into 2D Conductive Oxide Interfaces. *J Electroceram* (2017) 38:1–23. doi:10.1007/s10832-016-0051-0
50. Moetakef P, Cain TA, Ouellette DG, Zhang JY, Klenov DO, Janotti A, et al. Electrostatic Carrier Doping of $GdTiO_3/SrTiO_3$ Interfaces. *Appl Phys Lett* (2011) 99:232116. doi:10.1063/1.3669402
51. Xu P, Ayino Y, Cheng C, Pribiag VS, Comes RB, Sushko PV, et al. Predictive Control over Charge Density in the Two-Dimensional Electron Gas at the Polar-Nonpolar $NdTiO_3/SrTiO_3$ Interface. *Phys Rev Lett* (2016) 117:106083. doi:10.1103/PhysRevLett.117.106803
52. Nakagawa N, Hwang HY, and Muller DA. Why Some Interfaces Cannot Be Sharp. *Nat Mater* (2006) 5:204–9. doi:10.1038/nmat1569
53. Mannhart J, and Schlom DG. Oxide Interfaces-An Opportunity for Electronics. *Science* (2010) 327:1607–11. doi:10.1126/science.1181862
54. Schlom DG, and Mannhart J. Interface Takes Charge over Si. *Nat Mater* (2011) 10:168–9. doi:10.1038/nmat2965
55. Nazir S, and Yang K. First-Principles Characterization of the Critical Thickness for Forming Metallic States in Strained $LaAlO_3/SrTiO_3$(001) Heterostructure. *ACS Appl Mater Inter* (2014) 6:22351–8. doi:10.1021/am506336w
56. Mannhart J, Blank DHA, Hwang HY, Millis AJ, and Triscone J-M. Two-Dimensional Electron Gases at Oxide Interfaces. *MRS Bull* (2008) 33:1027–34. doi:10.1557/mrs2008.222
57. Rose MA, Smid B, Vorokhta M, Slipukhina I, Andra M, Bluhm H, et al. Identifying Ionic and Electronic Charge Transfer at Oxide Heterointerfaces. *Adv Mater Interfaces* (2020) 33:2004132. doi:10.1002/adma.202004132
58. Willmott PR, Pauli SA, Herger R, Schlepütz CM, Martoccia D, Patterson BD, et al. Structural Basis for the Conducting Interface between $LaAlO_3$ and $SrTiO_3$. *Phys Rev Lett* (2007) 99:1–4. doi:10.1103/PhysRevLett.99.155502
59. Shen J, Lee H, Valentí R, and Jeschke HO. Ab Initiostudy of the Two-Dimensional Metallic State at the Surface of $SrTiO_3$: Importance of Oxygen Vacancies. *Phys Rev B* (2012) 86:195119. doi:10.1103/PhysRevB.86.195119
60. Liu ZQ, Sun L, Huang Z, Li CJ, Zeng SW, Han K, et al. Dominant Role of Oxygen Vacancies in Electrical Properties of Unannealed $LaAlO_3/SrTiO_3$ Interfaces. *J Appl Phys* (2014) 115:054303. doi:10.1063/1.4863800
61. Liu ZQ, Li CJ, Lü WM, Huang XH, Huang Z, Zeng SW, et al. Origin of the Two-Dimensional Electron Gas at $LaAlO_3/SrTiO_3$ Interfaces: The Role of Oxygen Vacancies and Electronic Reconstruction. *Phys Rev X* (2013) 3:021010. doi:10.1103/PhysRevX.3.021010
62. Li Y, Wei X, and Yu J. Inevitable High Density of Oxygen Vacancies at the Surface of Polar-Nonpolar Perovskite Heterostructures $LaAlO_3/SrTiO_3$. *J Appl Phys* (2020) 127:205302. doi:10.1063/1.5128080
63. Yu L, and Zunger A. A Polarity-Induced Defect Mechanism for Conductivity and Magnetism at Polar-Nonpolar Oxide Interfaces. *Nat Commun* (2014) 5:1–9. doi:10.1038/ncomms6118
64. Zhang Y, Gan Y, Niu W, Norrman K, Yan X, Christensen DV, et al. Tuning the Two-Dimensional Electron Gas at Oxide Interfaces with Ti-O Configurations: Evidence from X-ray Photoelectron Spectroscopy. *ACS Appl Mater Inter* (2018) 10:1434–9. doi:10.1021/acsami.7b16510
65. Mauro C, Barone C, Di Gennaro E, Sambri A, Guarino A, Granozio FM, et al. Photoconductivity in 2D Electron Gases at the Amorphous-LGO/STO Oxide Interface: a Dynamical Analysis. *Eur Phys J Spec Top* (2019) 228:675–81. doi:10.1140/epjst/e2019-800168-y
66. Shibuya K, Ohnishi T, Lippmaa M, and Oshima M. Metallic Conductivity at the $CaHfO_3$/$SrTiO_3$ Interface. *Appl Phys Lett* (2007) 91:232106–8. doi:10.1063/1.2816907
67. Lee SW, Liu Y, Heo J, and Gordon RG. Creation and Control of Two-Dimensional Electron Gas Using Al-Based Amorphous Oxides/$SrTiO_3$ Heterostructures Grown by Atomic Layer Deposition. *Nano Lett* (2012) 12:4775–83. doi:10.1021/nl302214x
68. Lee SW, Heo J, and Gordon RG. Origin of the Self-Limited Electron Densities at $Al_2O_3/SrTiO_3$ Heterostructures Grown by Atomic Layer Deposition - Oxygen Diffusion Model. *Nanoscale* (2013) 5:8940–4. doi:10.1039/c3nr03082b
69. Lee HJ, Moon T, An CH, and Hwang CS. 2D Electron Gas at the Interface of Atomic-Layer-Deposited Al_2O_3/TiO_2 on $SrTiO_3$ Single Crystal Substrate. *Adv Electron Mater* (2019) 5:1800527. doi:10.1002/aelm.201800527
70. Kumah DP, Ngai JH, and Kornblum L. Epitaxial Oxides on Semiconductors: From Fundamentals to New Devices. *Adv Funct Mater* (2020) 30:1901597. doi:10.1002/adfm.201901597
71. Kornblum L, Jin EN, Shoron O, Boucherit M, Rajan S, Ahn CH, et al. Electronic Transport of Titanate Heterostructures and Their Potential as Channels on (001) Si. *J Appl Phys* (2015) 118:105301. doi:10.1063/1.4930140
72. Park JW, Bogorin DF, Cen C, Felker DA, Zhang Y, Nelson CT, et al. Creation of a Two-Dimensional Electron Gas at an Oxide Interface on Silicon. *Nat Commun* (2010) 1:1–7. doi:10.1038/ncomms1096
73. Edmondson BI, Liu S, Lu S, Wu H, Posadas A, Smith DJ, et al. Effect of $SrTiO_3$ Oxygen Vacancies on the Conductivity of $LaTiO_3/SrTiO_3$ Heterostructures. *J Appl Phys* (2018) 124:185303. doi:10.1063/1.5046081

74. Kornblum L, Faucher J, Morales-Acosta MD, Lee ML, Ahn CH, and Walker FJ. Oxide Heterostructures for High Density 2D Electron Gases on GaAs. *J Appl Phys* (2018) 123:025302. doi:10.1063/1.5004576
75. Zhang L, and Engel-Herbert R. Growth of $SrTiO_3$on Si(001) by Hybrid Molecular Beam Epitaxy. *Phys Status Solidi RRL* (2014) 8:917–23. doi:10.1002/pssr.201409383
76. Chen J-Y, Huang C-W, Chiu C-H, Huang Y-T, and Wu W-W. Switching Kinetic of VCM-Based Memristor: Evolution and Positioning of Nanofilament. *Adv Mater* (2015) 27:5028–33. doi:10.1002/adma.201502758
77. Pi S, Li C, Jiang H, Xia W, Xin H, Yang JJ, et al. Memristor Crossbar Arrays with 6-nm Half-Pitch and 2-nm Critical Dimension. *Nat Nanotech* (2018) 14: 35–9. doi:10.1038/s41565-018-0302-0
78. Ma X, Wu H, Wu D, and Qian H. A 16 Mb RRAM Test Chip Based on Analog Power System with Tunable Write Pulses In: 15th Non-Volatile Memory Technology Symposium (NVMTS). Piscataway, NJ: IEEE (2015) p. 1–3. doi:10.1109/NVMTS.2015.7457478
79. Yu S, Li Z, Chen P-Y, Wu H, Gao B, Wang D, Wu W, and Qian H. Binary Neural Network with 16 Mb RRAM Macro Chip for Classification and Online Training In: IEEE International Electron Devices Meeting (IEDM), Piscataway, NJ: IEEE (2016) 16–2. doi:10.1109/IEDM.2016.7838429
80. Hsu C, Wan C, Wang I, Chen M, Lo C, Lee Y, et al. 3D Vertical TaO_x/TiO_2 RRAM with over 10^3 Self-Rectifying Ratio and Sub-μa Operating Current. *IEDM Tech Dig - Int Electron Devices Meet* (2013) 2:264–7. doi:10.1109/IEDM.2013.6724601
81. Hsieh M-C, Liao Y-C, Chin Y-W, Lien C-H, Chang T-S, Chih Y-D, et al. Ultra High Density 3D via RRAM in Pure 28nm CMOS Process. *Tech Dig - Int Electron Devices Meet IEDM* (2013) 1:260–3. doi:10.1109/IEDM.2013.6724600
82. Yu S, Gao B, Fang Z, Yu H, Kang J, and Wong H-SP. A Neuromorphic Visual System Using RRAM Synaptic Devices with Sub-pJ Energy and Tolerance to Variability: Experimental Characterization and Large-Scale Modeling In: International electron devices meeting (IEMD). Piscataway, NJ: IEEE (2012) p. 10–4. doi:10.1109/LED.2012.221085610.1109/iedm.2012.6479018
83. Torrezan AC, Strachan JP, Medeiros-Ribeiro G, and Williams RS. Sub-nanosecond Switching of a Tantalum Oxide Memristor. *Nanotechnology* (2011) 22:485203. doi:10.1088/0957-4484/22/48/485203
84. Valov I, Waser R, Jameson JR, and Kozicki MN. Electrochemical Metallization Memories-Fundamentals, Applications, Prospects. *Nanotechnology* (2011) 22:289502. doi:10.1088/0957-4484/22/28/289502
85. Yang Y, and Lu WD. Progress in the Characterizations and Understanding of Conducting Filaments in Resistive Switching Devices. *IEEE Trans Nanotechnology* (2016) 15:465–72. doi:10.1109/TNANO.2016.2544782
86. Yang Y, Gao P, Gaba S, Chang T, Pan X, and Lu W. Observation of Conducting Filament Growth in Nanoscale Resistive Memories. *Nat Commun* (2012) 3:732–8. doi:10.1038/ncomms1737
87. Wu SX, Peng HY, and Wu T. Concurrent Nonvolatile Resistance and Capacitance Switching in $LaAlO_3$. *Appl Phys Lett* (2011) 98:093503. doi:10.1063/1.3560257
88. Wei Z, Kanzawa Y, Arita K, Katoh Y, Kawai K, Muraoka S, et al. Highly Reliable TaO_x ReRAM and Direct Evidence of Redox Reaction Mechanism. *IEEE Int Electron Devices Meet* (2008) 1–4. doi:10.1109/IEDM.2008.4796676
89. Miron D, Krylov I, Baskin M, Yalon E, and Kornblum L. Understanding Leakage Currents through Al_2O_3 on $SrTiO_3$. *J Appl Phys* (2019) 126:185301. doi:10.1063/1.5119703
90. Wu Y, Yu S, Lee B, and Wong P. Low-power TiN/Al_2O_3/Pt Resistive Switching Device with Sub-20 μA Switching Current and Gradual Resistance Modulation. *J Appl Phys* (2011) 110:094104. doi:10.1063/1.3657938
91. Sarkar B, Lee B, and Misra V. Understanding the Gradual Reset in Pt/Al_2O_3/Ni RRAM for Synaptic Applications. *Semicond Sci Technol* (2015) 30:105014. doi:10.1088/0268-1242/30/10/105014
92. Su C, Shan L, Yang D, Zhao Y, Fu Y, Liu J, et al. Microelectronic Engineering Effects of Heavy Ion Irradiation on Cu/Al_2O_3/Pt CBRAM Devices. *Microelectron Eng* (2021) 247:111600. doi:10.1016/j.mee.2021.111600
93. Attarimashalkoubeh B, Prakash A, Lee S, Song J, Woo J, Misha SH, et al. Effects of Ti Buffer Layer on Retention and Electrical Characteristics of Cu-Based Conductive-Bridge Random Access Memory (CBRAM). *ECS Solid State Lett* (2014) 3:P120–P122. doi:10.1149/2.0031410ssl
94. Wu Y, Yu S, Wong HSP, Chen YS, Lee HY, Wang SM, Gu PY, Chen F, and Tsai MJ. AlO_x-based Resistive Switching Device with Gradual Resistance Modulation for Neuromorphic Device Application. 2012 4th IEEE International Memory Workshop, Milan, Italy: IEEE (2012) p. 1–4. doi:10.1109/IMW.2012.6213663
95. Liu K, Tzeng W, Chang K, Huang J, Lee Y, Yeh P, et al. Investigation of the Effect of Different Oxygen Partial Pressure to $LaAlO_3$ Thin Film Properties and Resistive Switching Characteristics. *Thin Solid Films* (2011) 520:1246–50. doi:10.1016/j.tsf.2011.04.205
96. Kim S, Biju KP, Jo M, Jung S, Park J, Lee J, et al. Effect of Scaling WO_x-Based RRAMs on Their Resistive Switching Characteristics. *IEEE Electron Device Lett* (2011) 32:671–3. doi:10.1109/LED.2011.2114320
97. Writam B, Xiaoxin X, Hangbing L, Qi L, Shibing L, and Ming L. Variability Improvement of TiO_x/Al_2O_3 Bilayer Nonvolatile Resistive Switching Devices by Interfacial Band Engineering with an Ultrathin Al_2O_3 Dielectric Material. *ACS OMEGA* (2017) 2:6888–95. doi:10.1021/acsomega.7b01211
98. Bousoulas P, Asenov P, Karageorgiou I, Sakellaropoulos D, Stathopoulos S, and Tsoukalas D. Engineering Amorphous-Crystalline Interfaces in TiO_{2-x}/TiO_{2-Y}-Based Bilayer Structures for Enhanced Resistive Switching and Synaptic Properties. *J Appl Phys* (2019) 120:154501. doi:10.1063/1.4964872
99. Branden L, Yibo L, and Rashmi J. Switching Characteristics of Ru/HfO_2/TiO_{2-x}/Ru RRAM Devices for Digital and Analog Nonvolatile Memory Applications. *IEEE Electron Device Lett* (2012) 33:706–8. doi:10.1109/LED.2012.2188775
100. Cheng CH, Albert C, and Yeh FS. Novel Ultra-low Power RRAM with Good Endurance and Retention. *Dig Tech Pap - Symp VLSI Technol* (2010) 85–6. doi:10.1109/VLSIT.2010.5556180
101. Schneider CW, Thiel S, Hammerl G, Richter C, and Mannhart J. Microlithography of Electron Gases Formed at Interfaces in Oxide Heterostructures. *Appl Phys Lett* (2006) 89:122101. doi:10.1063/1.2354422
102. Banerjee N, Huijben M, Koster G, and Rijnders G. Direct Patterning of Functional Interfaces in Oxide Heterostructures. *Appl Phys Lett* (2012) 100: 041601. doi:10.1063/1.3679379
103. Anders VB, Merlin von S, Ricci E, Rasmus Tindal D, Yu Z, Yulin G, et al. Nanoscale Patterning of Electronic Devices at the Amorphous $LaAlO_3$/$SrTiO_3$ Oxide Interface Using an Electron Sensitive Polymer Mask. *Appl Phys Lett* (2018) 112:171606. doi:10.1063/1.5026362

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