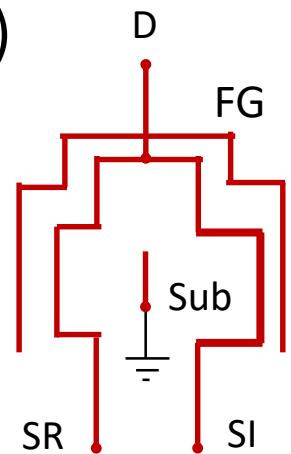
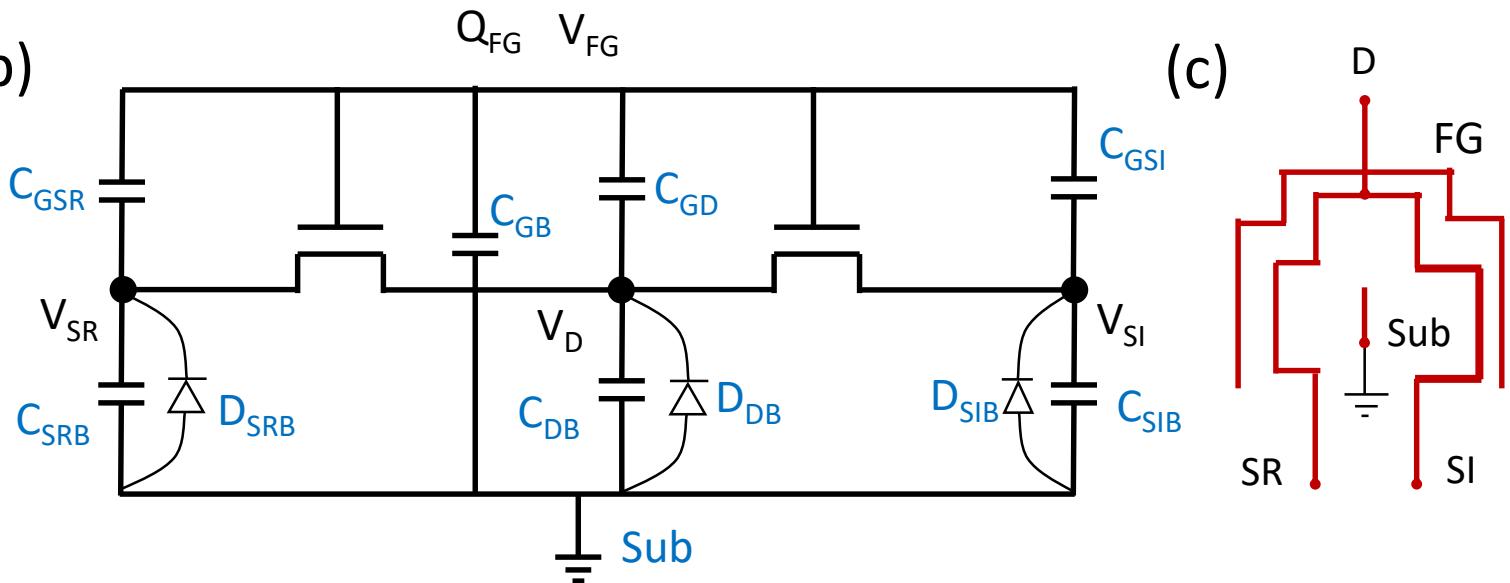
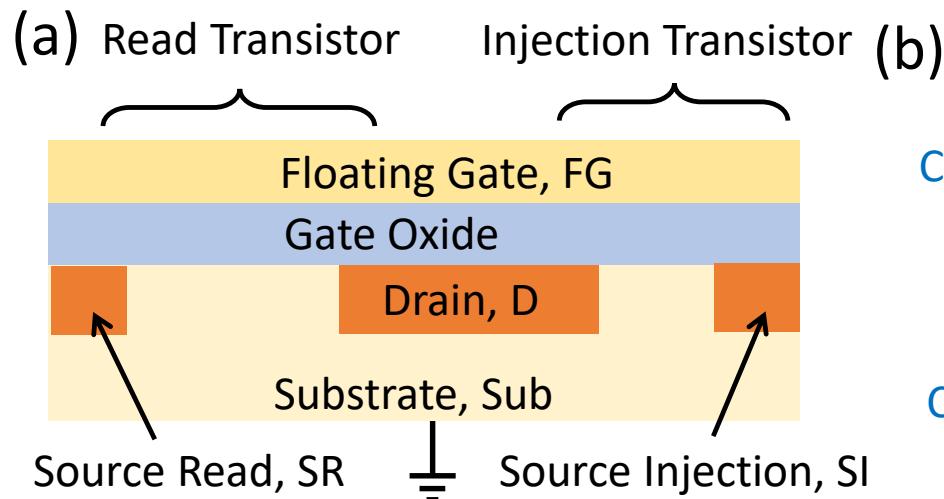


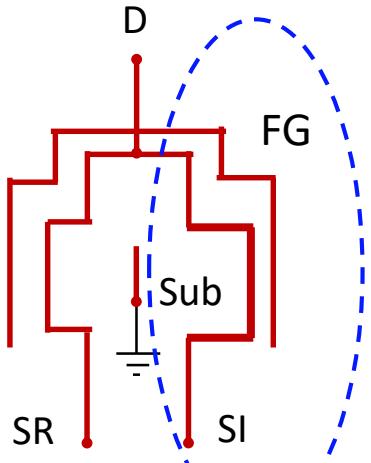
Y-Flash data analysis and device modelling

-- Wei Wang

➤ The capacitor network for voltage coupling



➤ Model for the transistors – Source/Drain/Gate current



- $V_{FG} - V_{TH} < 0$, Subthreshold region

$$I_{S,sub} = I_{S0} e^{\frac{q(V_{FG}-V_{TH})}{nkT}} (1 - e^{-\frac{q(V_D-V_S)}{kT}})$$

- $0 < V_{FG} - V_{TH} < V_D - V_S$, Saturation region

$$I_{S,ab} = \frac{K}{2} (V_{FG} - V_{TH})^2$$

- $V_{FG} - V_{TH} > V_D - V_S$, Linear region

$$I_{S,ab} = K \left(V_{FG} - V_{TH} - \frac{V_D - V_S}{2} \right) (V_D - V_S)$$

$$I_S = \left(\frac{1}{I_{S,sub}^m} + \frac{1}{I_{S,ab}^m} \right)^{-\frac{1}{m}}$$

$$I_{S0} = \frac{W}{L} \alpha_e C_{ox}^* \left(\frac{kT}{q} \right)^2 (n - 1)$$

$$K = \frac{W}{L} \mu C_{ox}$$

- For readout transistor:

$$V_{TH} = V_{TH,r}, K = K_r, I_{S0} = I_{SR0}, V_S = V_{SR} \quad \xrightarrow{I_{SR}}$$

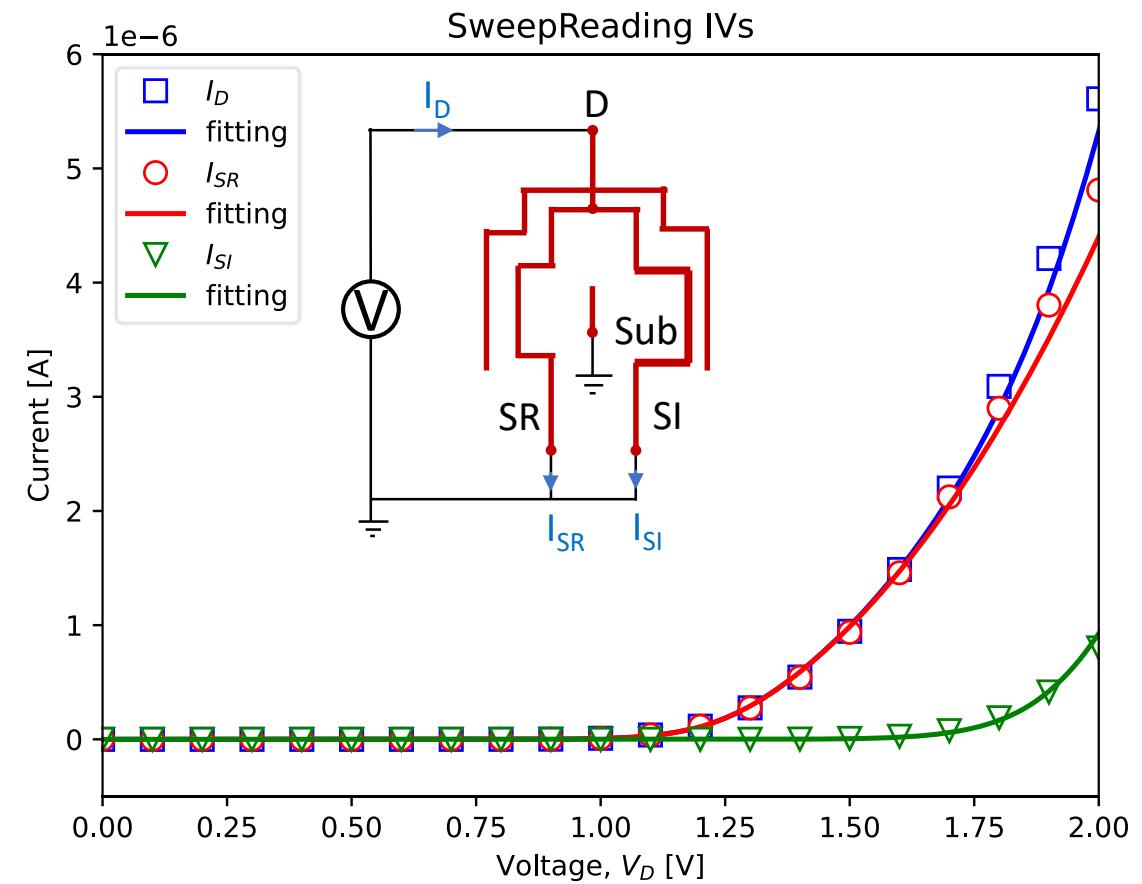
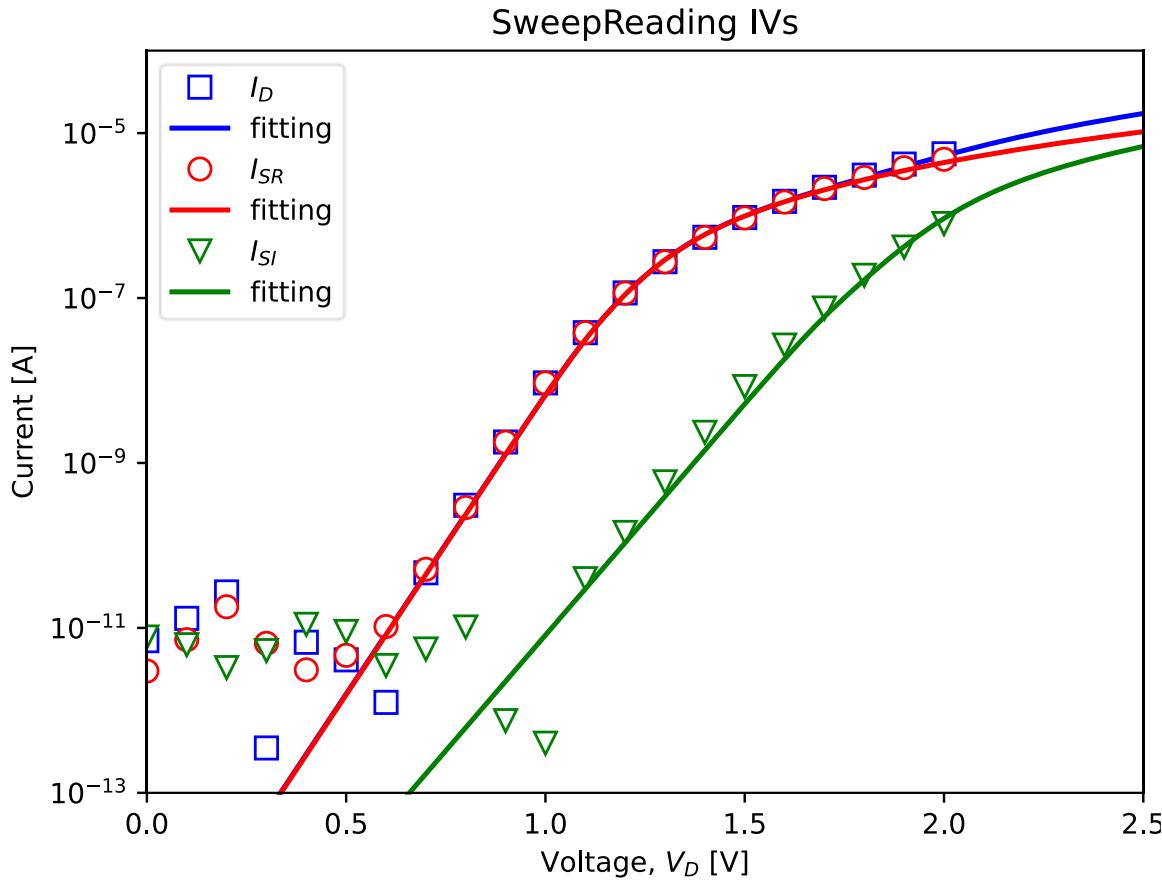
- For injection transistor:

$$V_{TH} = V_{TH,i}, K = K_i, I_{S0} = I_{SI0}, V_S = V_{SI} \quad \xrightarrow{I_{SI}}$$

$$I_D = I_{SR} + I_{SI}$$

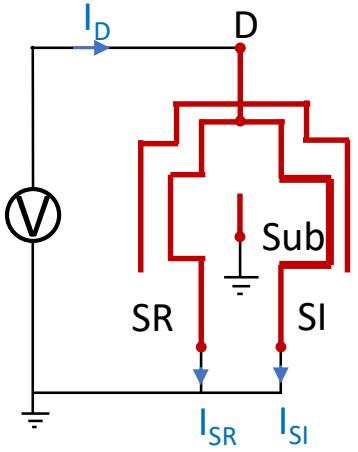
$$V_{TH,r} < V_{TH,i}, K_i = 2K_r$$

➤ IV curves for reading in Subthreshold and Normal region

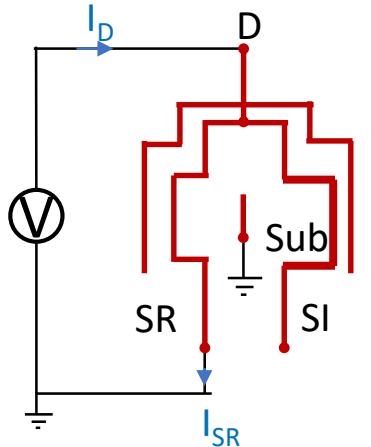


➤ IV curves for reading: more reading modes

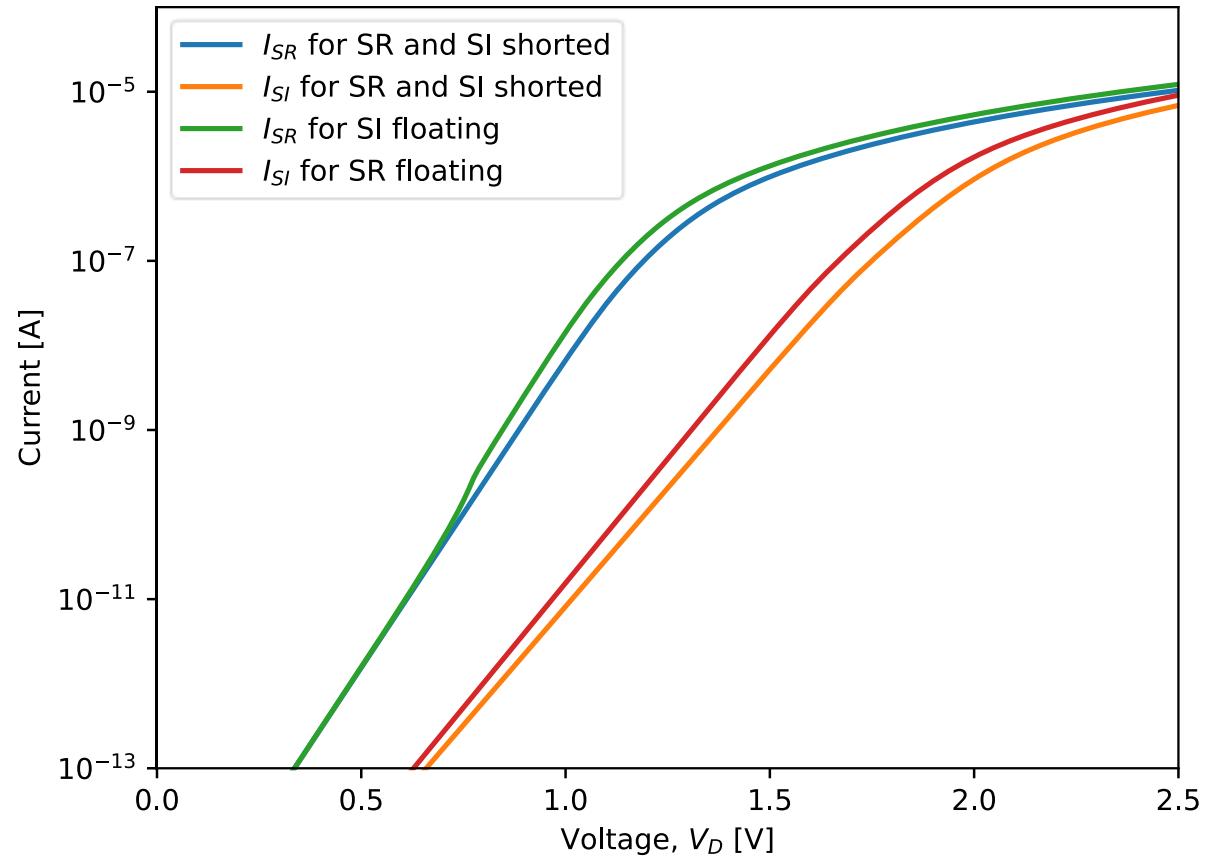
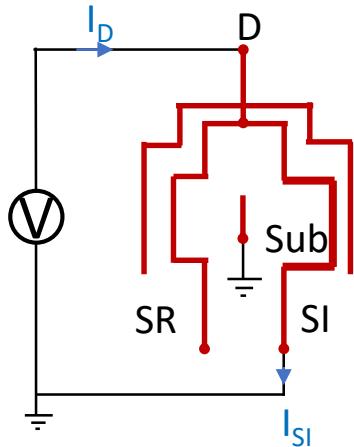
Mode 1: SR and SI shorted



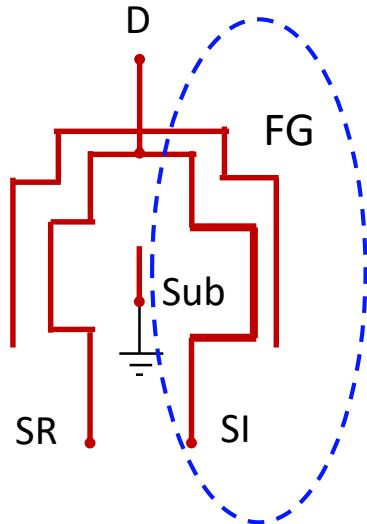
Mode 2: SI floating



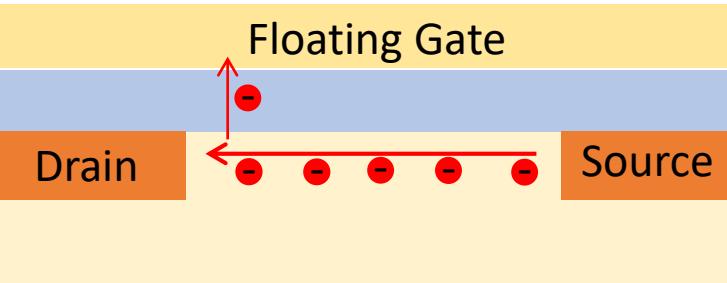
Mode 3: SI floating



➤ Program and Erase mechanism - Current from/to the floating gate

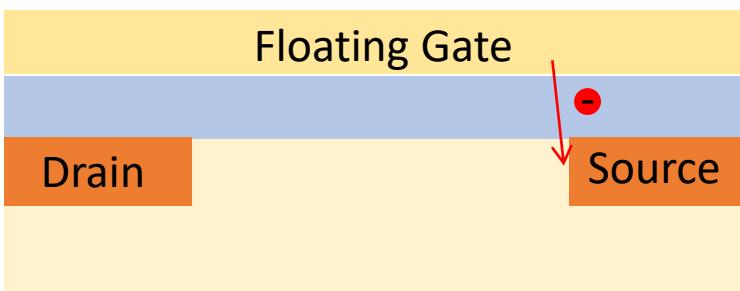


➤ Channel hot electron injection (lucky electron)



- Happens only in the injection transistor

➤ Tunnel electron



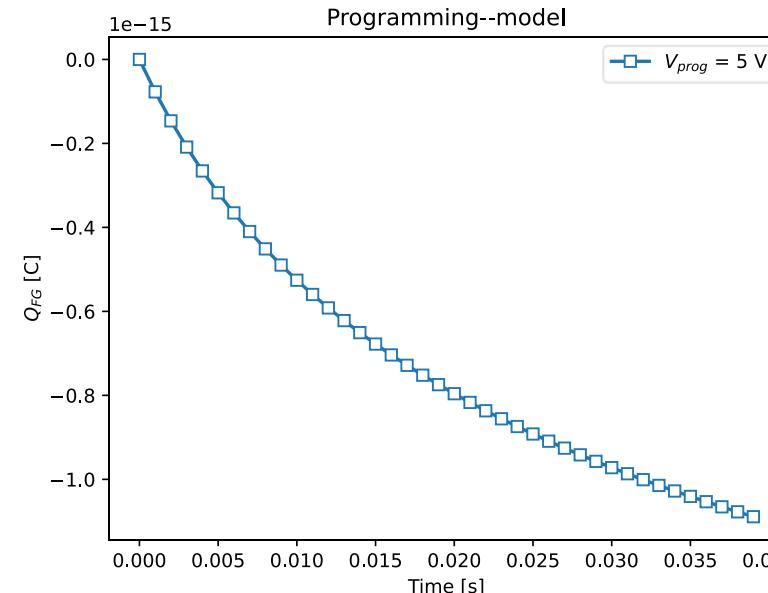
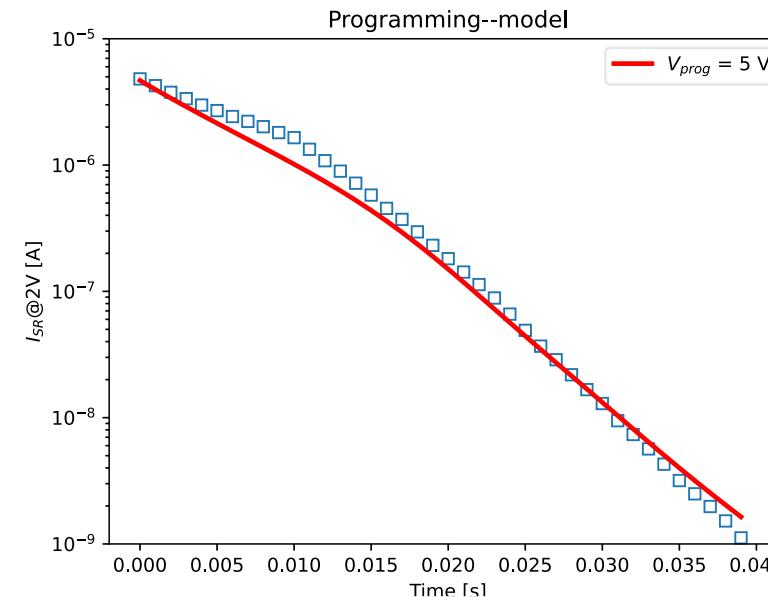
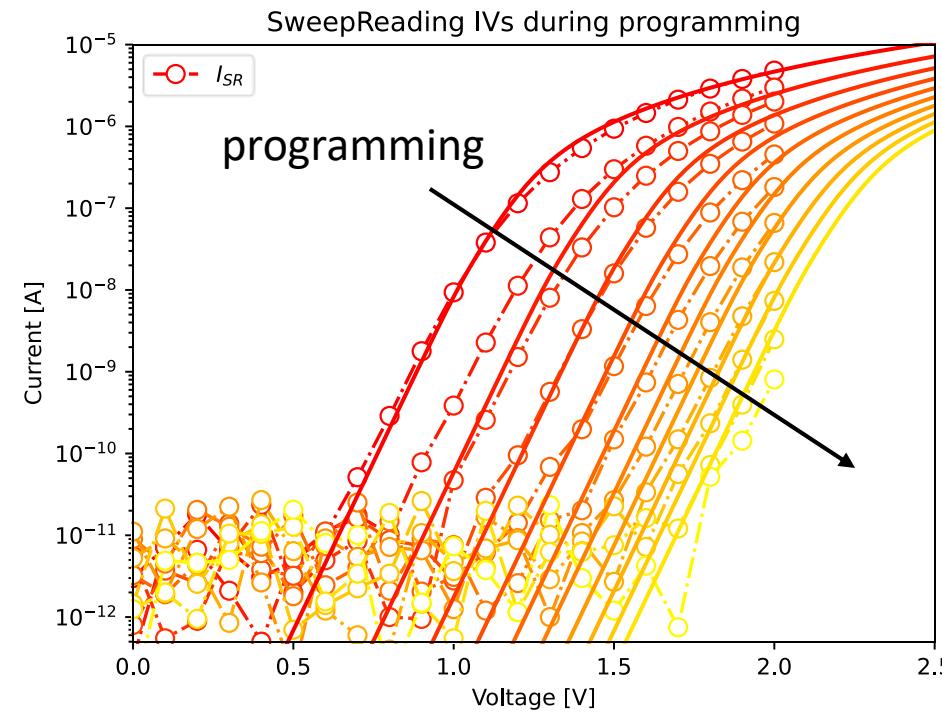
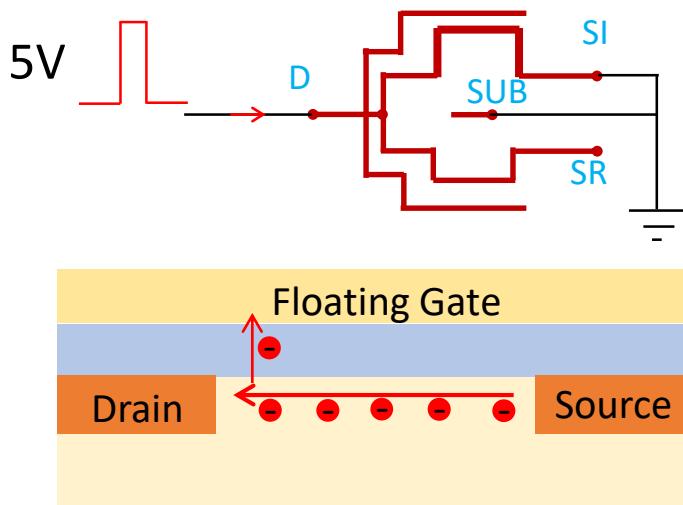
- Happens on both transistor

➤ Total gate current

$$I_G = \underbrace{\xi(V_{FG} - V_{bi})^2 e^{-\frac{\beta}{V_{FG}-V_{bi}}}}_{\text{Tunnelling current}} - \underbrace{I_S P_0 e^{-\frac{V_\alpha}{V_{FG}}}}_{\text{Injection current}}$$

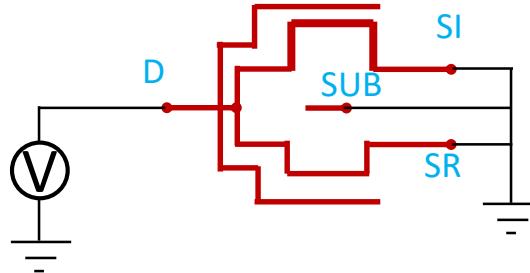
$$\frac{dQ_{FG}}{dt} = I_G$$

➤ IV reading during programming

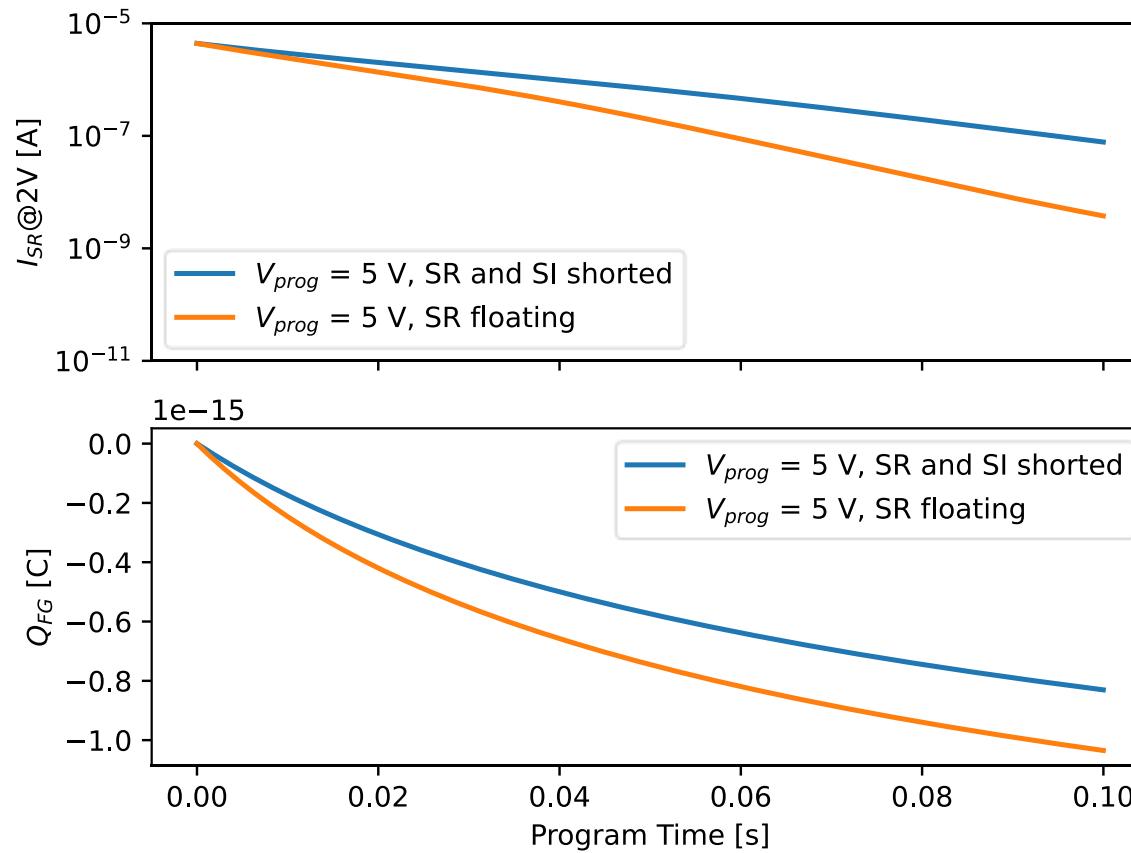
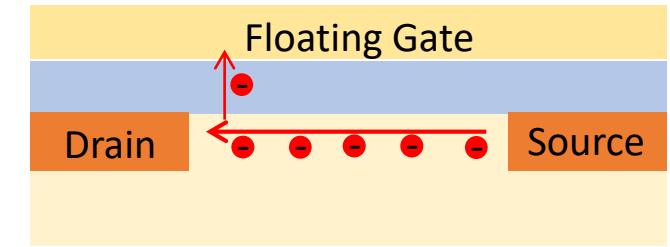
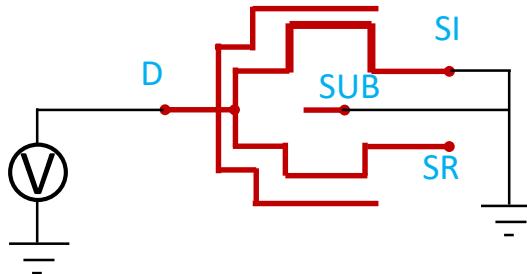


➤ More program modes

- Mode 1: SI and SR shorted



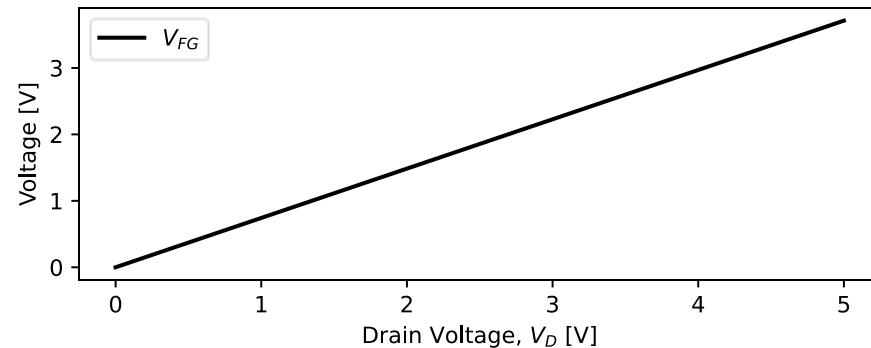
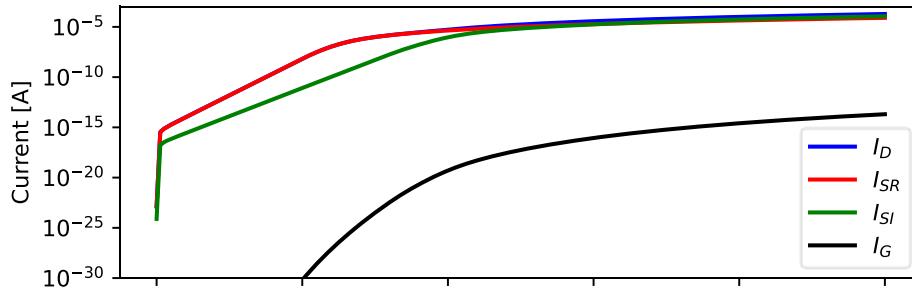
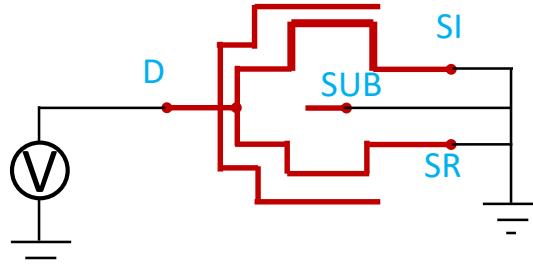
- Mode 2: SR floating



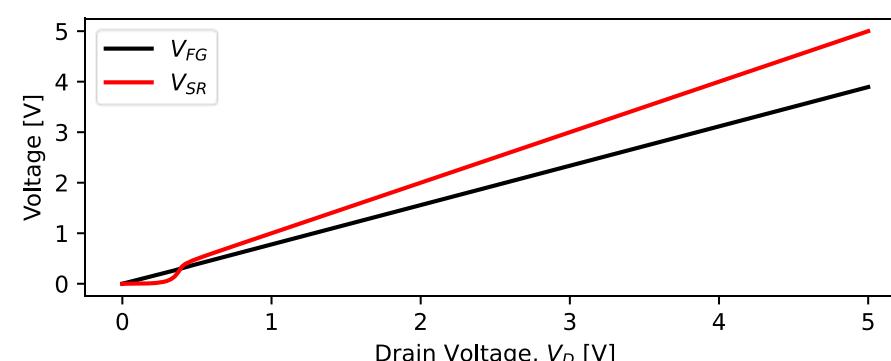
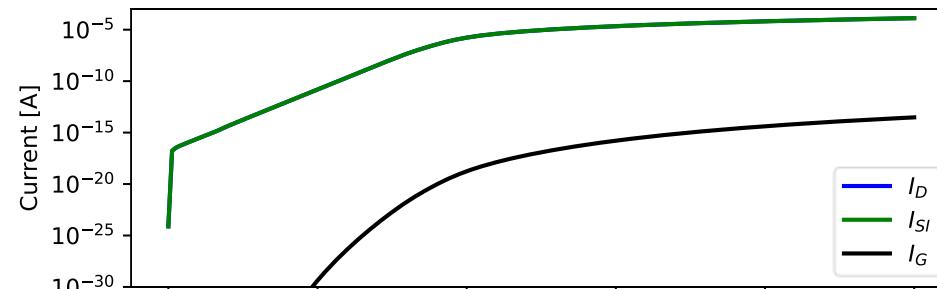
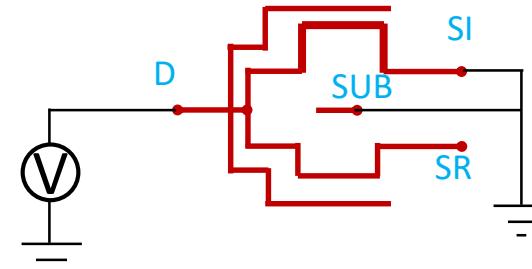
➤ Mode 2 is slightly more efficient than Mode 1

➤ More program modes

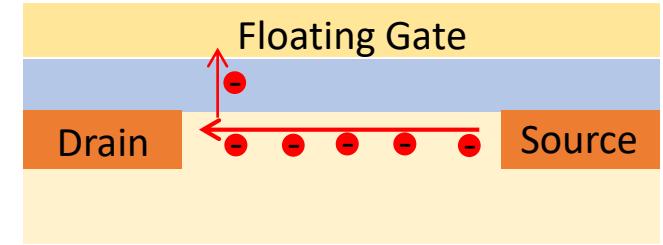
- Mode 1: SI and SR shorted



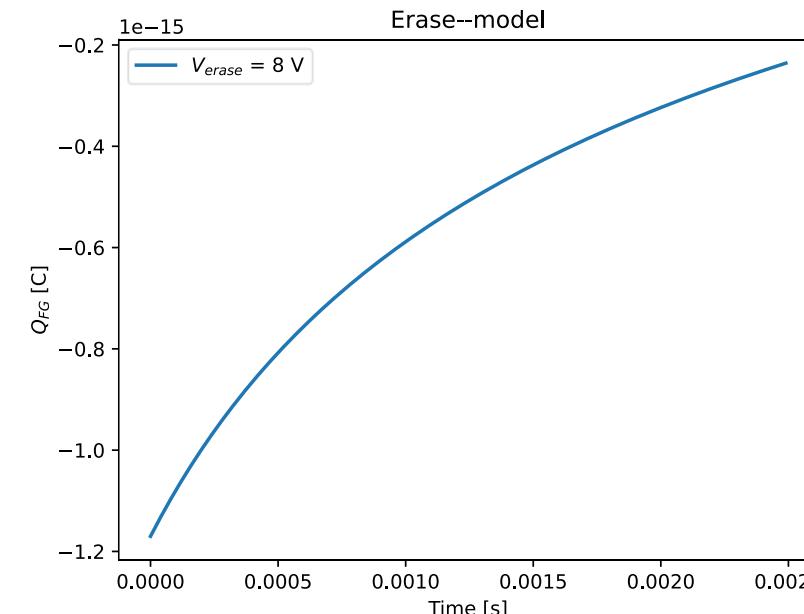
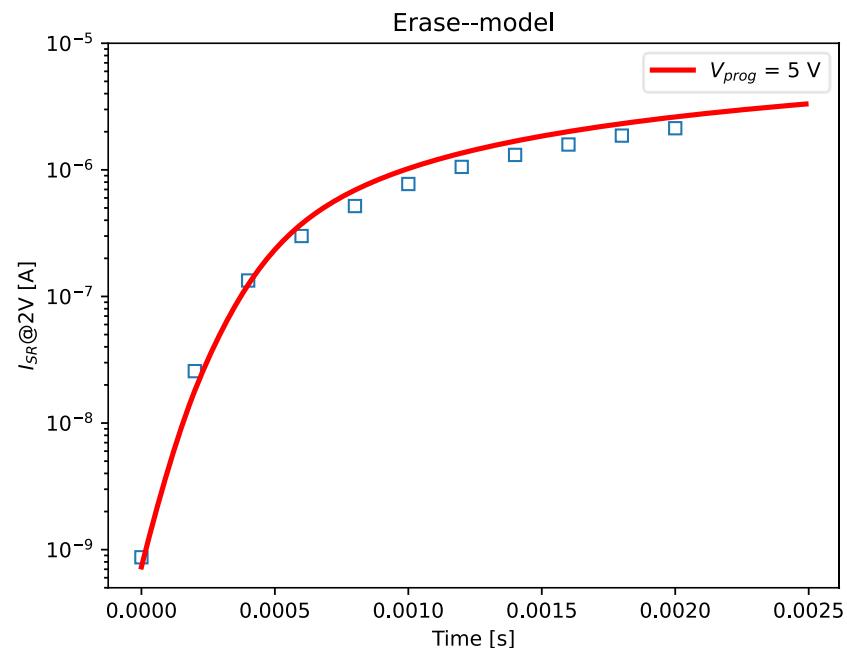
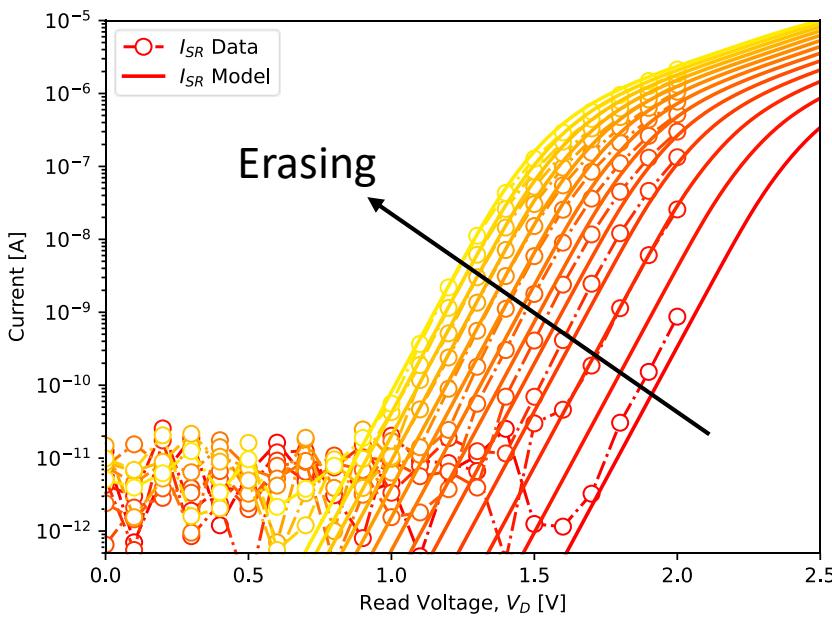
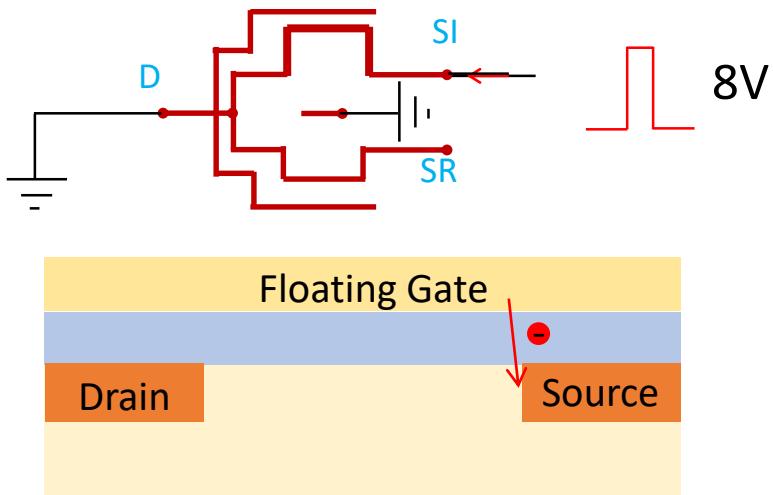
- Mode 2: SR floating



➤ Mode 2 is slightly more efficient than Mode 1

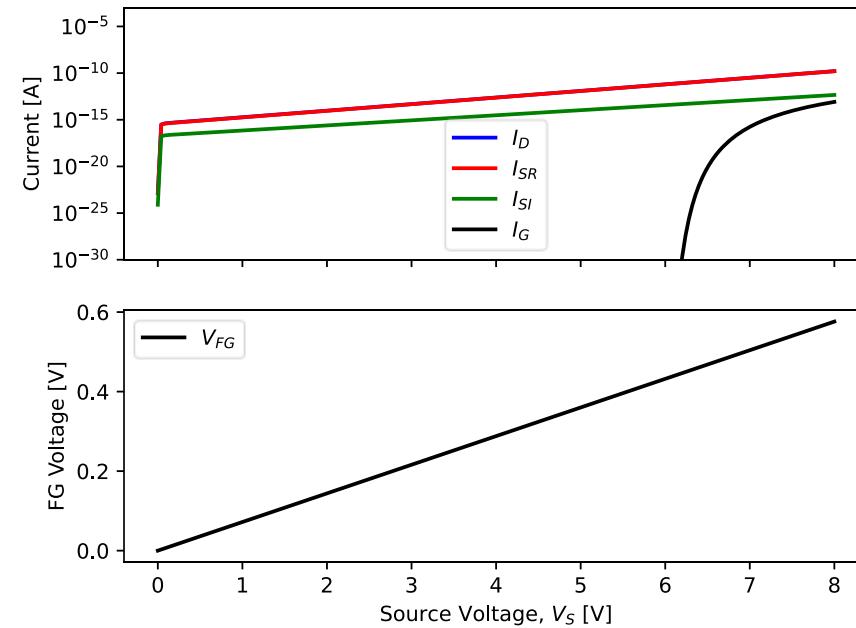
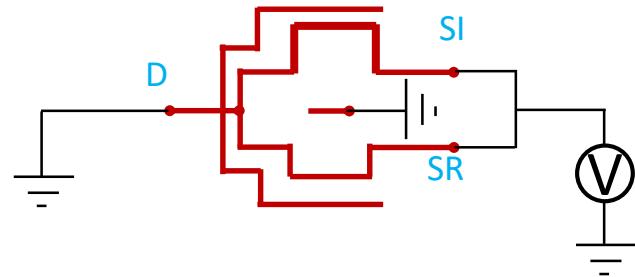


➤ IV reading curves during erasing

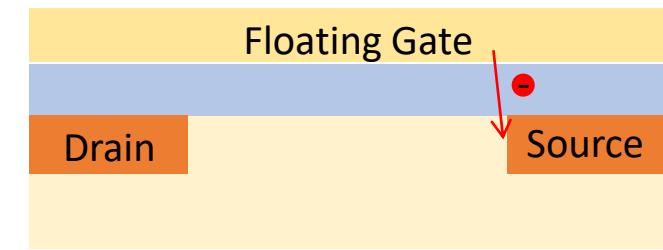
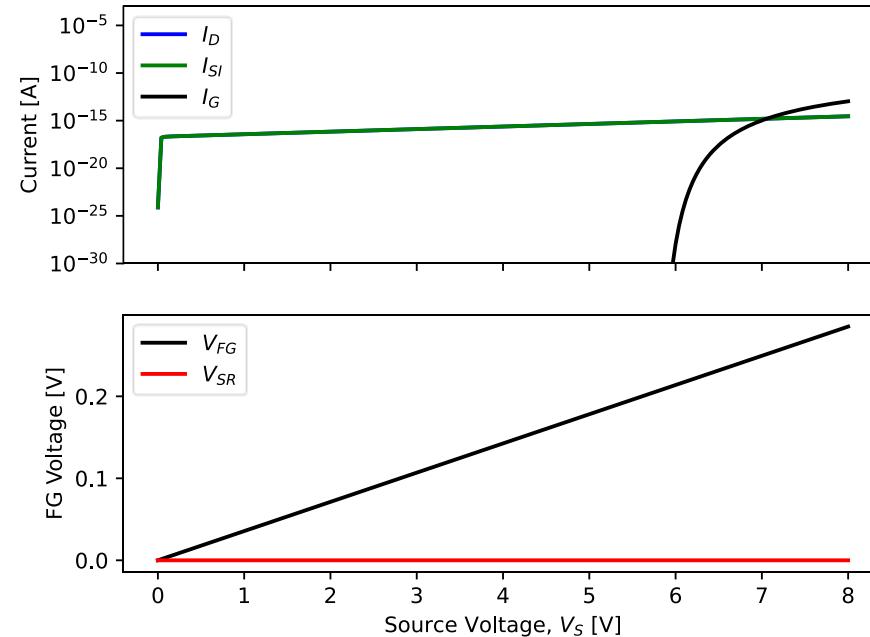
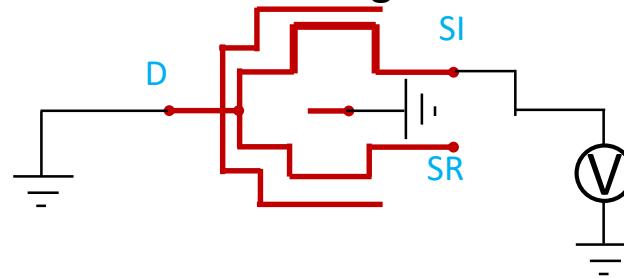


➤ More erase modes

- Mode 1: SI and SR shorted



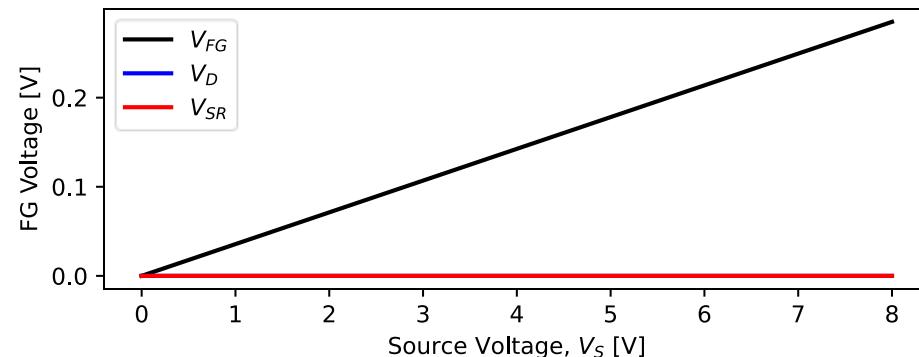
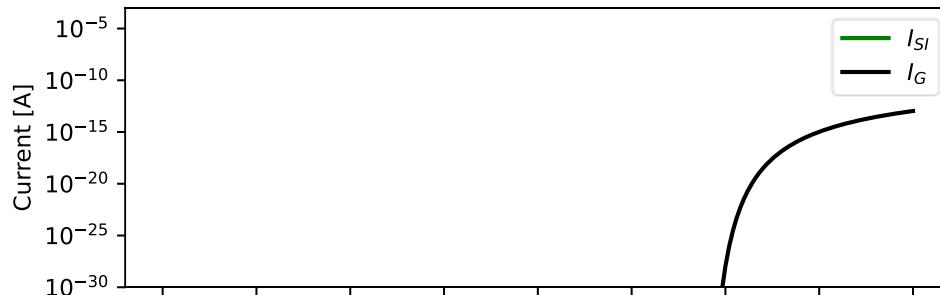
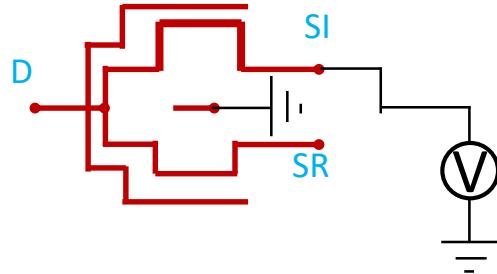
- Mode 2: SR floating



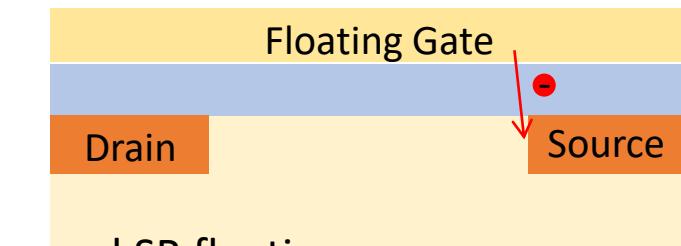
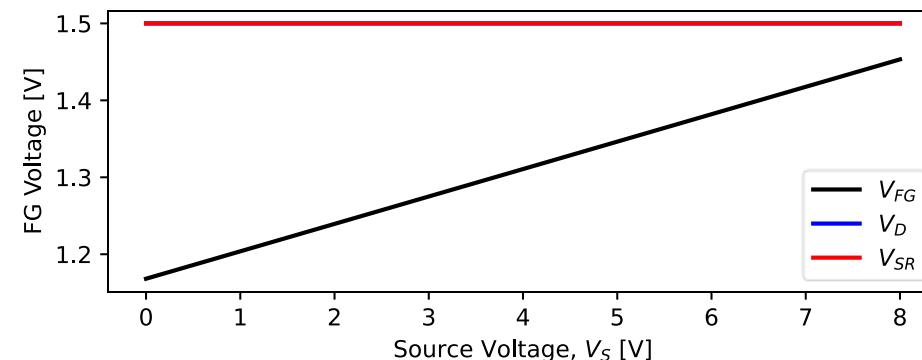
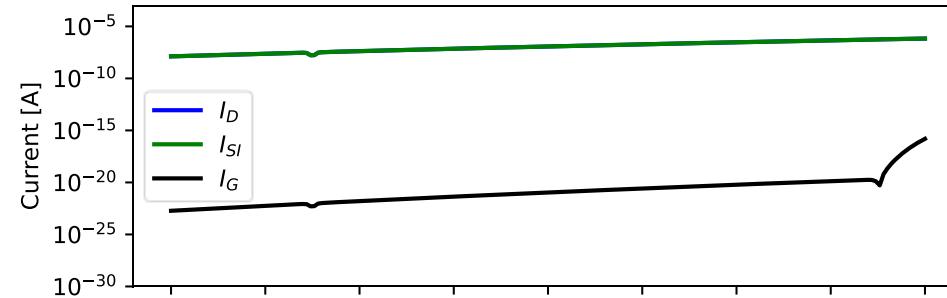
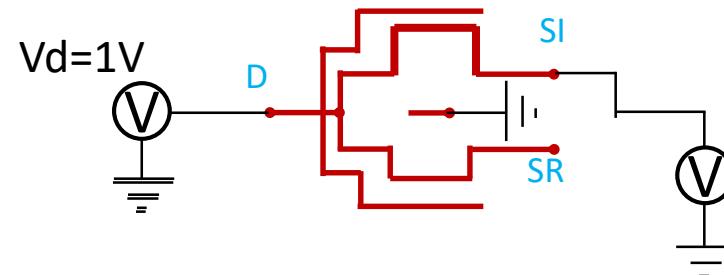
➤ Mode 2 is slightly more efficient than Mode 1

➤ More erase modes

- Mode 3: D and SR floating

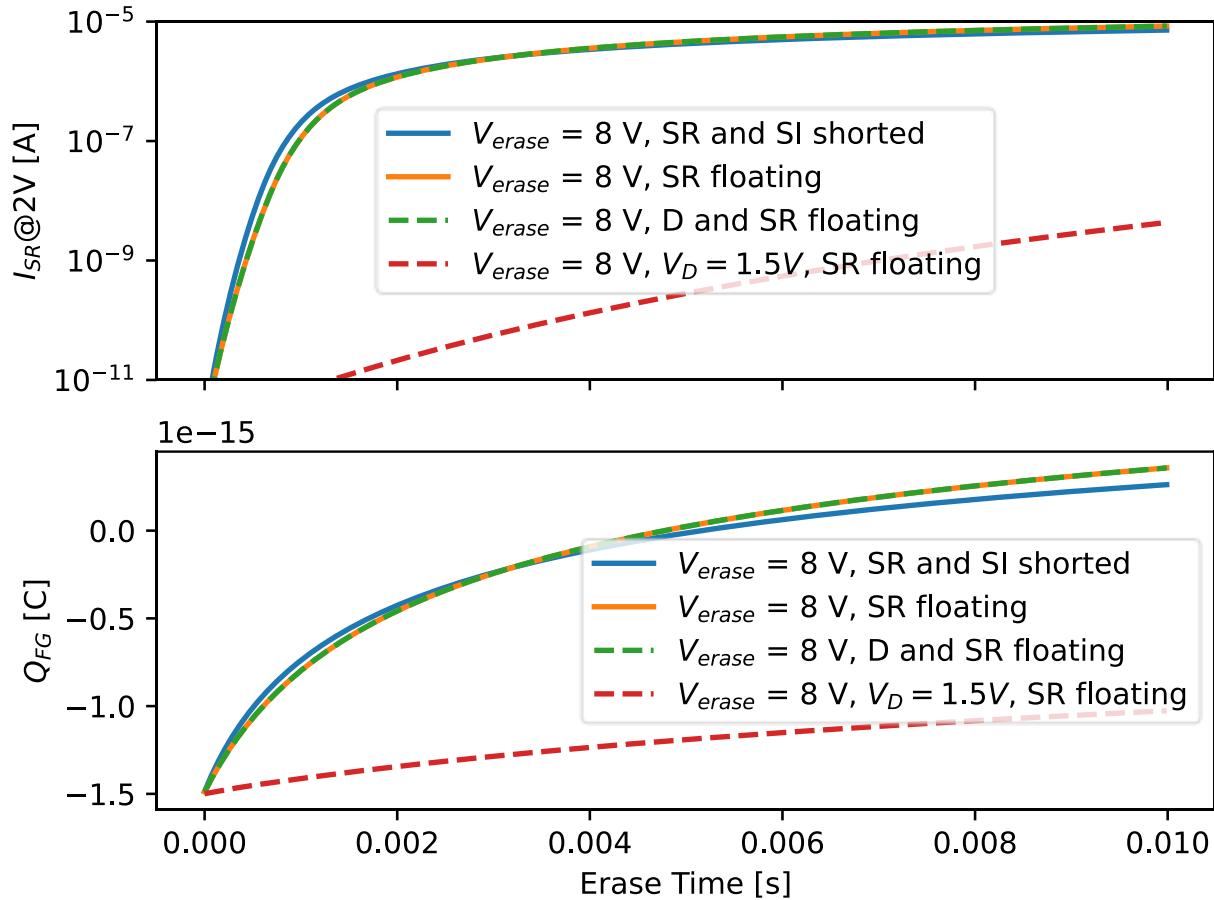
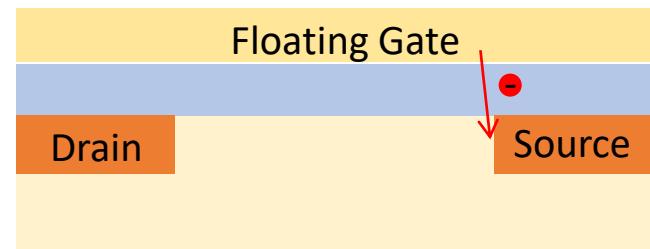


- Mode 4: A small voltage on Drain, and SR floating

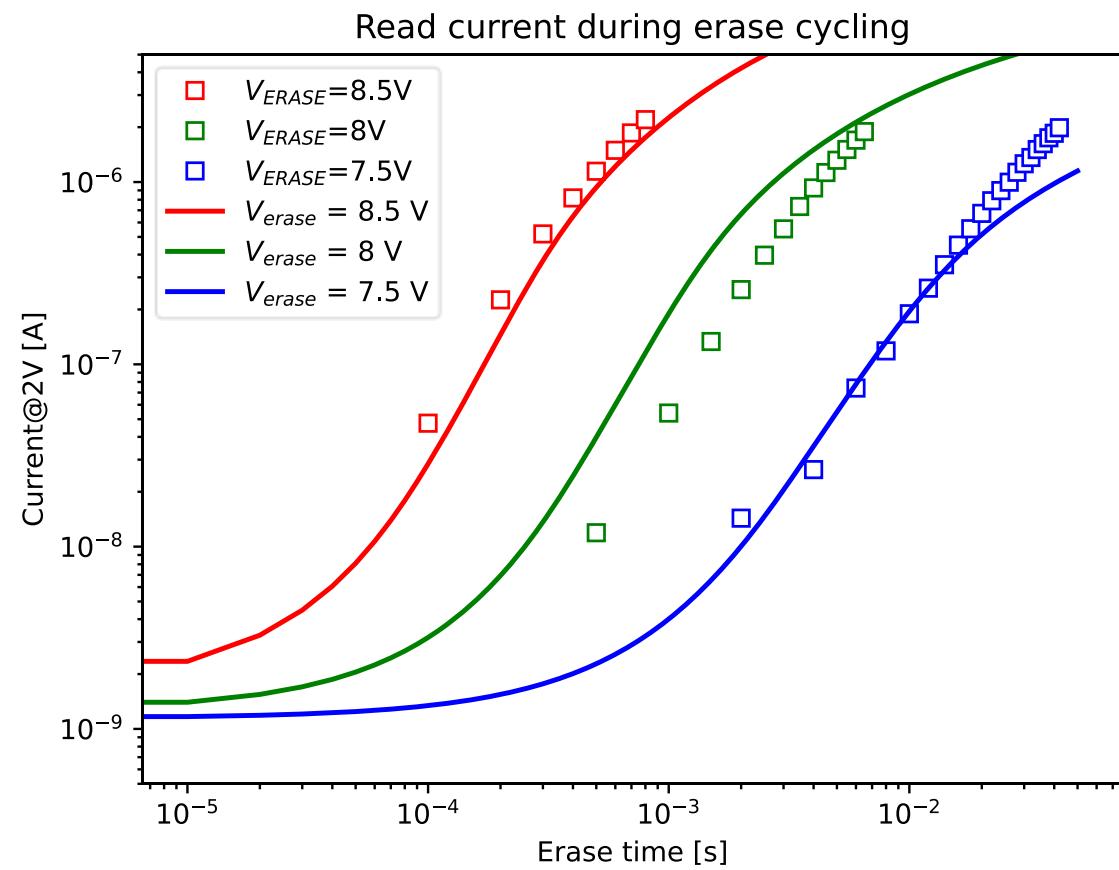
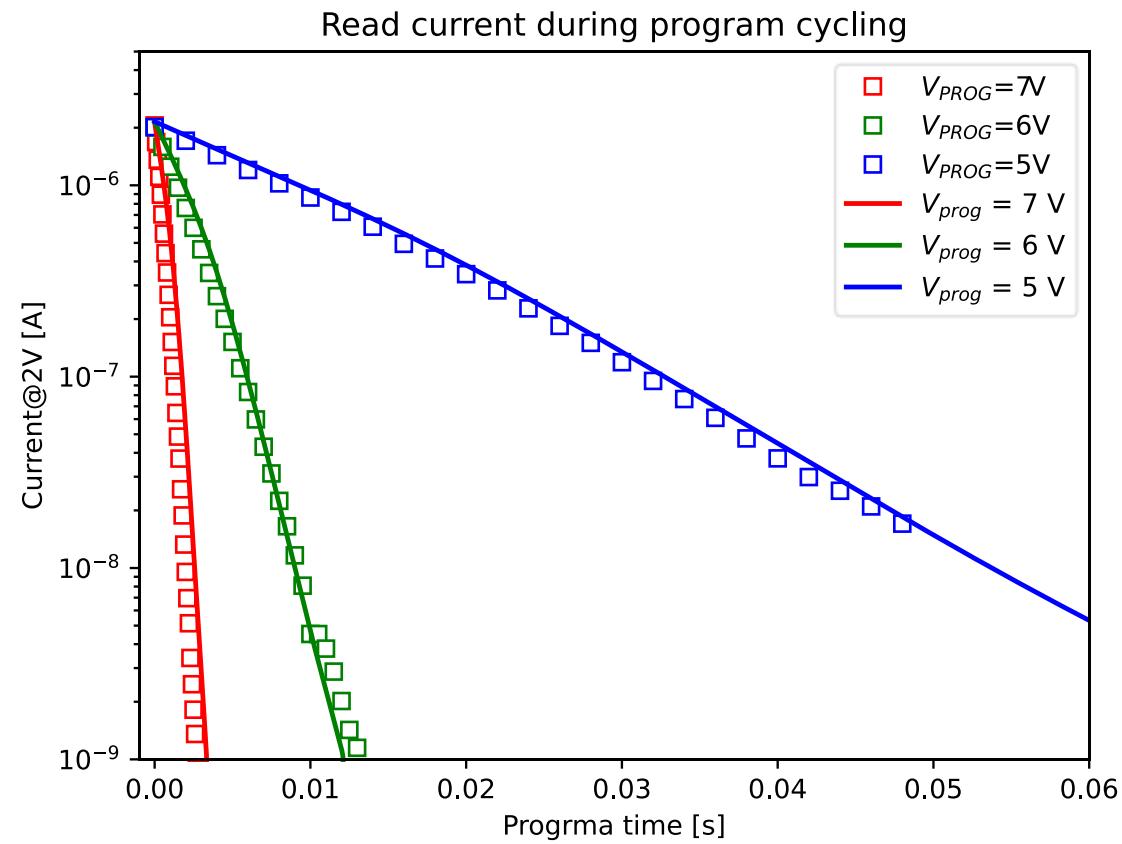


- Whether Drain is floating or grounded does not matter much
- Applying a small voltage on Drain can prevent Erase

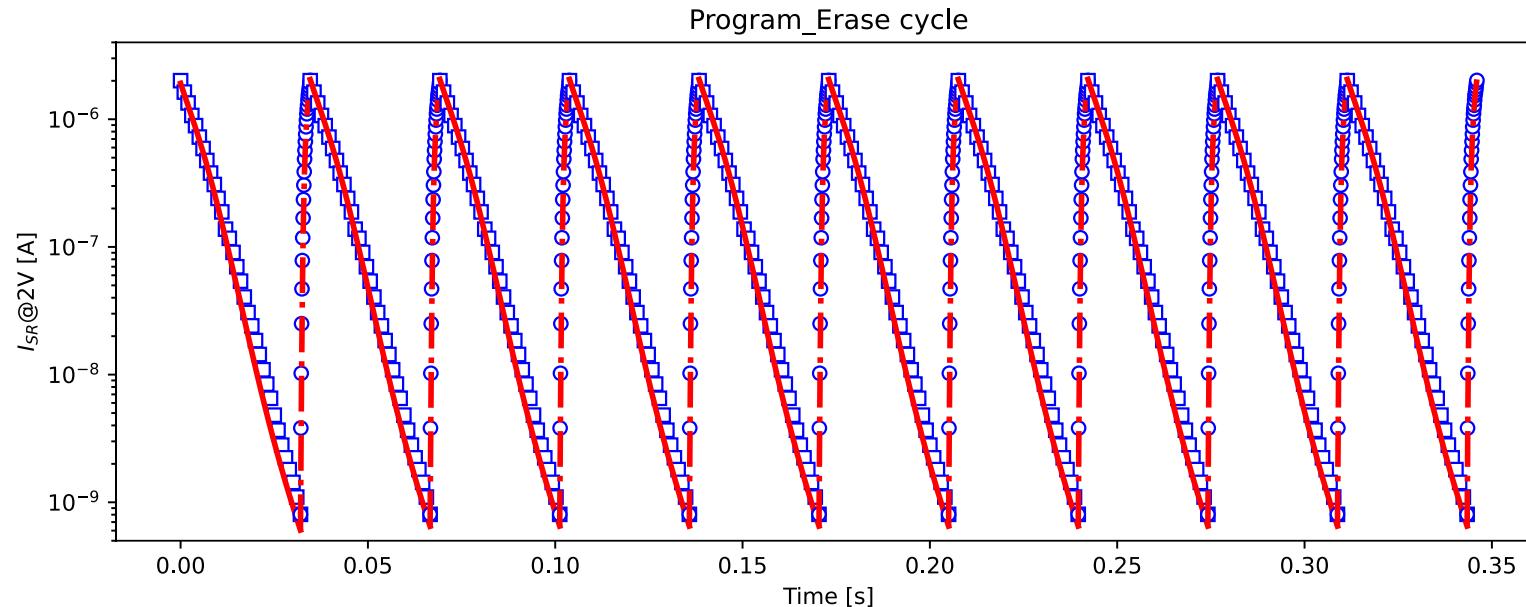
➤ More erase modes



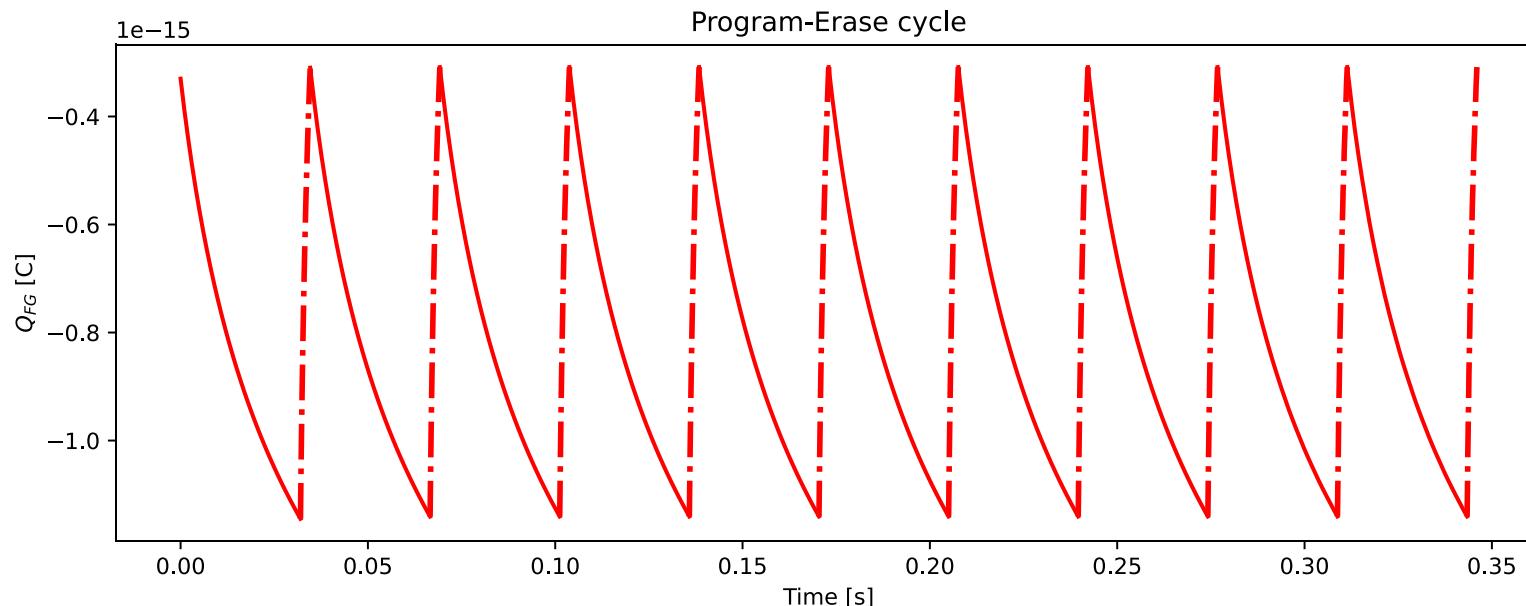
➤ Program and erase at different voltages



➤ Cycling of the program and erase operations

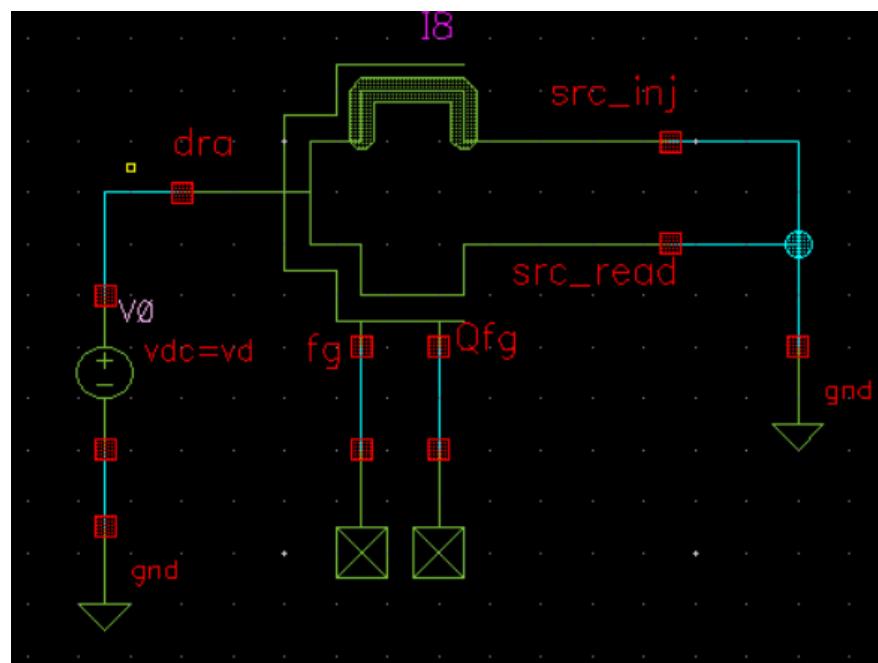


- Data vs. Model



- Up to 100 cycle data are available

➤ Verilog-a Model - 1



```
// VerilogA for Y_Flash, veriloga
// wei 20210511

`include "constants.vams"
`include "disciplines.vams"

discipline Chrg
    potential Charge;
enddiscipline

module y_flash (src_read, src_inj, dra, fg, Qfg);

    inout src_read, src_inj, dra;
    output fg, Qfg; //outputs only for monitoring the state of the devices

    electrical src_read, src_inj, dra;
    electrical fg, fg_d; //floating gate and dummy floating gate
    Chrg Qfg;           //self defined discipline for charge in the floating gate
    ground gnd;         //substrate of the device is always grounded

    //PARAMETERS
    parameter real Qfg_ini = 0 from [-5e-15:1e-15];
    //Parasitic Capacitors [from Loai D. Nat. Elect., 2, 596 (2019).]
    parameter real Cgd = 1.0e-15;
    parameter real Cgsr = 0.049e-15;
    parameter real Cgsi = 0.048e-15;
    parameter real Cdb = 0.64e-15;
    parameter real Cgb = 0.24e-15;
    //Parameters for readout transistor
    parameter real r_Vth = 0.82;
    parameter real r_K = 1.9e-5;
    parameter real r_Is0 = 4e-8;
    parameter real r_n = 1.7;
    parameter real r_Prob0 = 0;
    parameter real r_Va = 0;
    parameter real r_beta = 10;
    parameter real r_Vbi = 5.5;
    parameter real r_xi = 2e-12;
    //Parameters for injection transistor
    parameter real i_Vth = 0.82+0.52;
    parameter real i_K = 1.9e-5*2;
    parameter real i_Is0 = 4e-8*2;
    parameter real i_n = 1.7*1.3;
    parameter real i_Prob0 = 3.9e-8;
    parameter real i_Va = 20;
    parameter real i_beta = 10;
```

➤ Verilog-a Model - 2

```

parameter real r_Va      = 0;
parameter real r_beta    = 10;
parameter real r_Vbi     = 5.5;
parameter real r_xi      = 2e-12;
//Parameters for injection transistor
parameter real i_Vth     = 0.82+0.52;
parameter real i_K       = 1.9e-5*2;
parameter real i_Is0     = 4e-8*2;
parameter real i_n       = 1.7*1.3;
parameter real i_Prob0   = 3.9e-8;
parameter real i_Va      = 20;
parameter real i_beta    = 10;
parameter real i_Vbi     = 5.5;
parameter real i_xi      = 2.0e-12;

////////////////// MAIN //////////////////

// Instances of the two transistors: read transistor and injection transistor
Transistorfg #(.Vth(r_Vth), .K(r_K), .Is0(r_Is0), .n(r_n), .Prob0(r_Prob0), .Va(r_Va), .beta(r_beta), .Vbi(r_Vbi), .xi(r_xi)) Source_Read(.g(fg_d), .dra(dra), .src(src_read));
Transistorfg #(.Vth(i_Vth), .K(i_K), .Is0(i_Is0), .n(i_n), .Prob0(i_Prob0), .Va(i_Va), .beta(i_beta), .Vbi(i_Vbi), .xi(i_xi)) Source_Inj(.g(fg_d), .dra(dra), .src(src_inj));

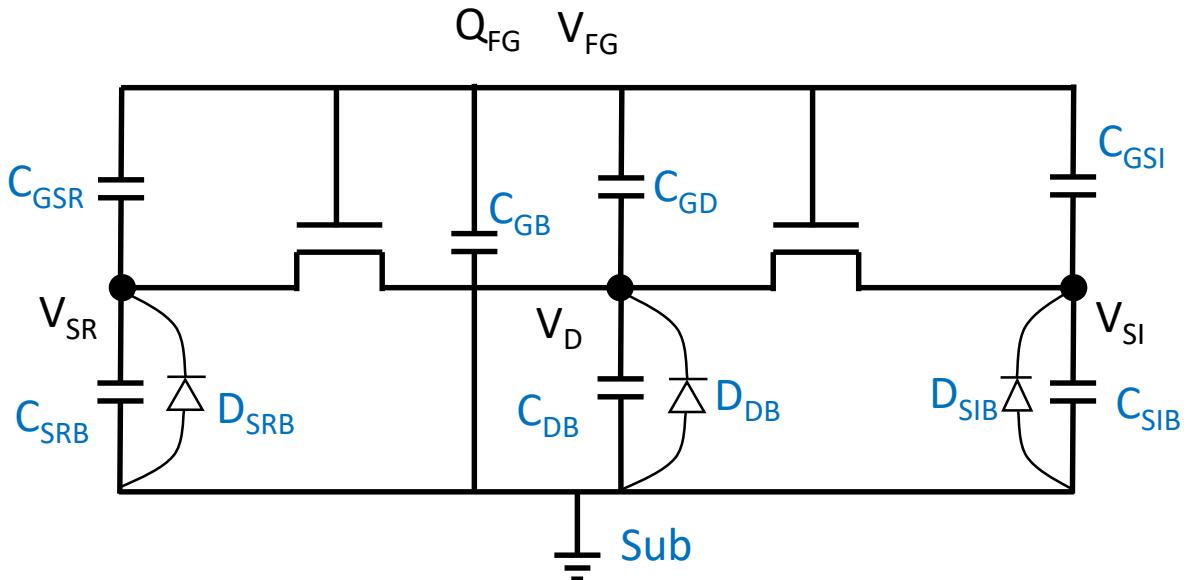
// PN-Junction Diodes between the terminals and substrates (there are also parasitic capacitor and resistor in the PN junctions)
PNDiode #(.Area(1), .Cjo(Cdb))      DRdgnd(.p(gnd), .n(dra));
PNDiode #(.Area(0.05), .Cjo(0.05*Cdb)) DRsrgnd(.p(gnd), .n(src_read));
PNDiode #(.Area(0.05), .Cjo(0.05*Cdb)) DRsignd(.p(gnd), .n(src_inj));

analog begin
    //the floating gate node does not follow KCL. A dummy floating point was employed to collect the gate current from the transistors (program and erase currents).
    //integrate the gate current in the floating gate
    V(fg_d) <+ V(fg);
    Q(Qfg) <+ idt(I(fg_d), Qfg_ini);
    V(fg) <+ (Q(Qfg)+Cgsr*V(src_read,gnd)+Cgd*V(dra,gnd)+Cgsi*V(src_inj,gnd))/(Cgsr+Cgd+Cgsi+Cgb);

    //Additional Capacitors can be seen from input terminals, affecting the transient behaviors
    I(dra,fg) <+ Cgd*dt(V(dra,fg));
    I(src_read,fg) <+ Cgsr*dt(V(src_read,fg));
    I(src_inj,fg) <+ Cgsi*dt(V(src_inj,fg));

    // $monitor("Time %f ms, Qfg=%f fC, Vfg= %f V",$realtime*1e3, Q(Qfg)*1e15, V(fg));
end
endmodule

```



➤ Verilog-a Model - 3

```
module Transistorfg(g,dra,src);
    inout g, dra, src; // gate, drain, source
    electrical g, dra, src;
    ground gnd;       // substrate

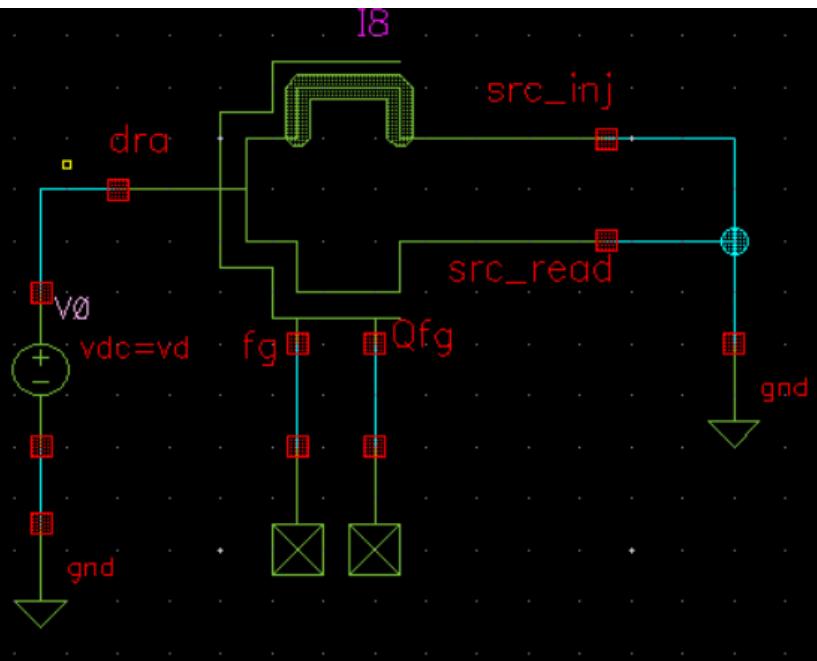
    //parameters for readout
    parameter real Vth = 0.85;
    parameter real K = 1.2e-5;
    parameter real Is0 = 2e-8;
    parameter real n = 1.7;
    //parameters for channel hot electron current
    parameter real Prob0 = 3.9e-8;
    parameter real Va = 20;
    //parameters for tunneling current
    parameter real beta = 10;
    parameter real Vbi = 5.5;
    parameter real xi = 2.0e-12;
    parameter real kT = $vt;

    //internal variables
    real Vds, Vgs;
    real Vsg;
    real is,is_sub,is_ab,igs_t,igs_l,igs; //current
    real m=1, s=5;

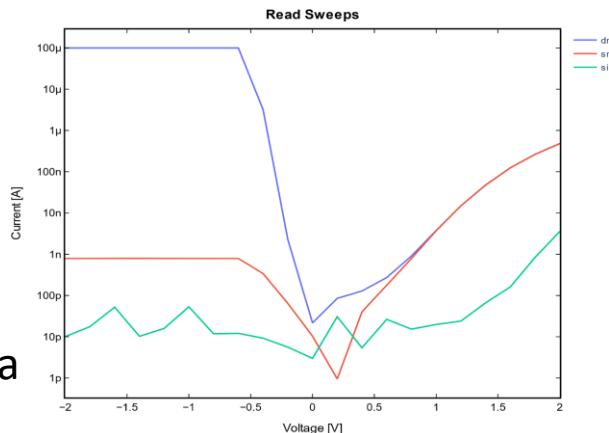
    analog begin
        // current of the readout transistor
        if (V(dra,gnd) == V(src,gnd))
            is = 0;
        else begin
            Vds = abs(V(dra)-V(src));
            if (V(dra)>V(src))
                Vgs=V(g)-V(src);
            else
                Vgs=V(g)-V(dra);
            is_sub = Is0*exp((Vgs-Vth)/(n*kT))*(1-exp(-Vds/kT));
            is_ab = s*Is0*(1-exp(-Vds/kT));
            if (Vgs-Vth >= 0) begin
                if (V(g)-Vth < Vds)
                    is_ab = is_ab + K/2*(Vgs - Vth)**2;
                else
                    is_ab = is_ab + K*(Vgs - Vth-Vds)*Vds;
            end
            is = (1/(1/(is_sub*m)+1/(is_ab*m)))**(1/m);
            if (V(dra)<V(src))
                is=-is;
        end
    end
    // lucky electron gate current
    if (V(g)<0.1)
        igs_l = 0;
    else
        igs_l=abs(is)*Prob0*exp(-Va/V(g));
    // tunneling gate current
    Vsg=V(src)-V(g);
    if (Vsg<Vbi)
        igs_t = 0;
    else
        igs_t = -xi*(Vsg-Vbi)**2*exp(-beta/(Vsg-Vbi));
    // total gate current in the readout transistor
    igs=igs_l+igs_t;
    I(dra,src) <+ is;
    I(g,src) <+ igs;
end
endmodule
```

➤ Verilog-a Model Results - 1

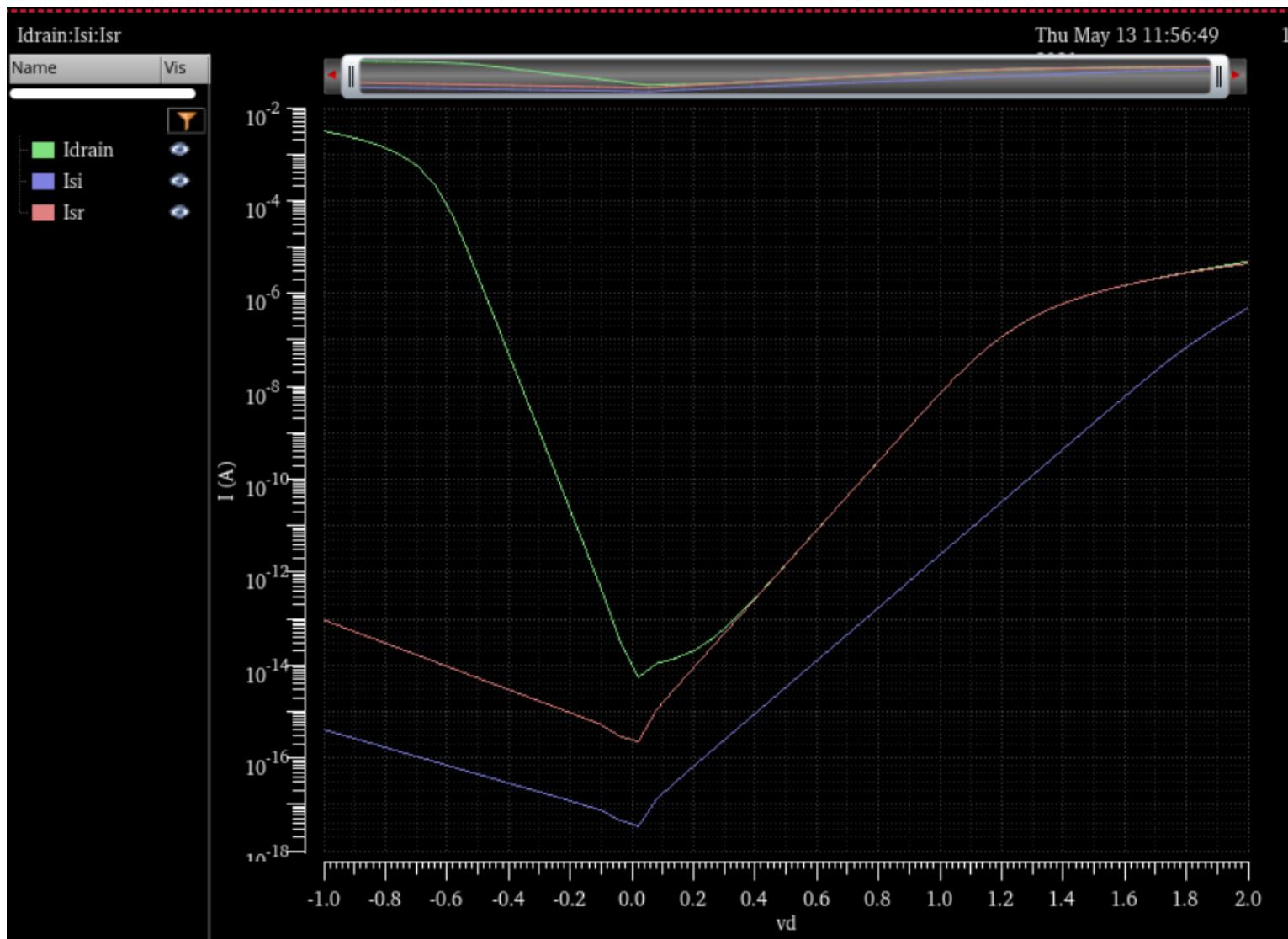
- DC Reading



$$Qfg = 0$$

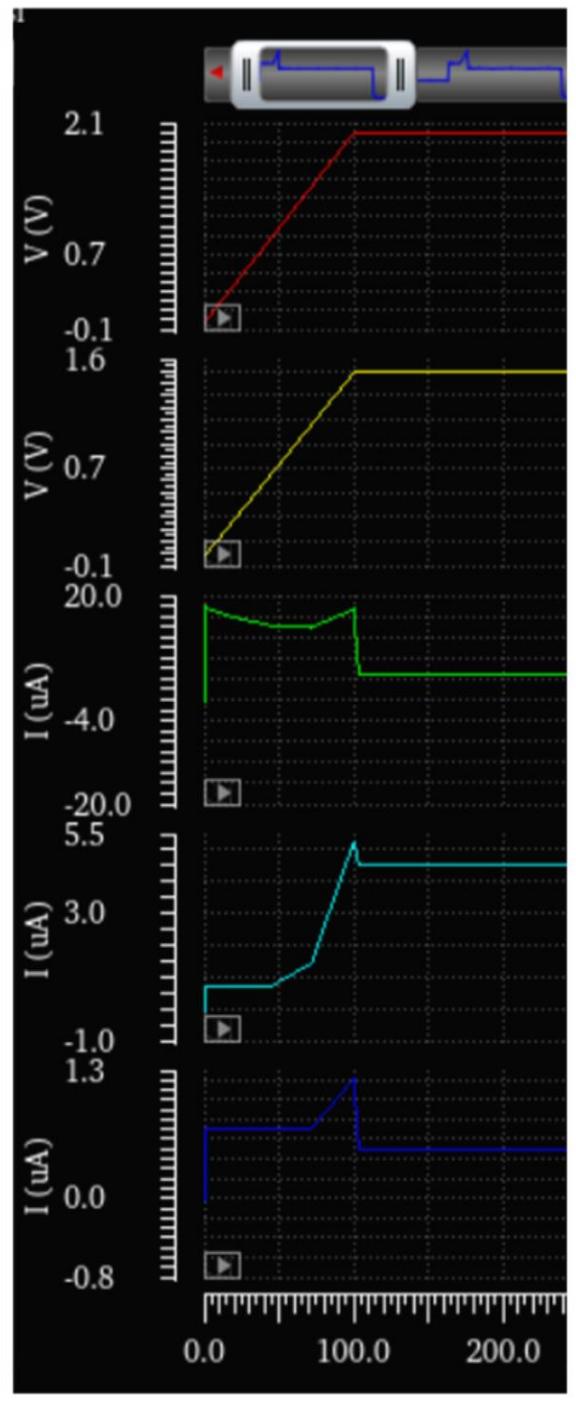
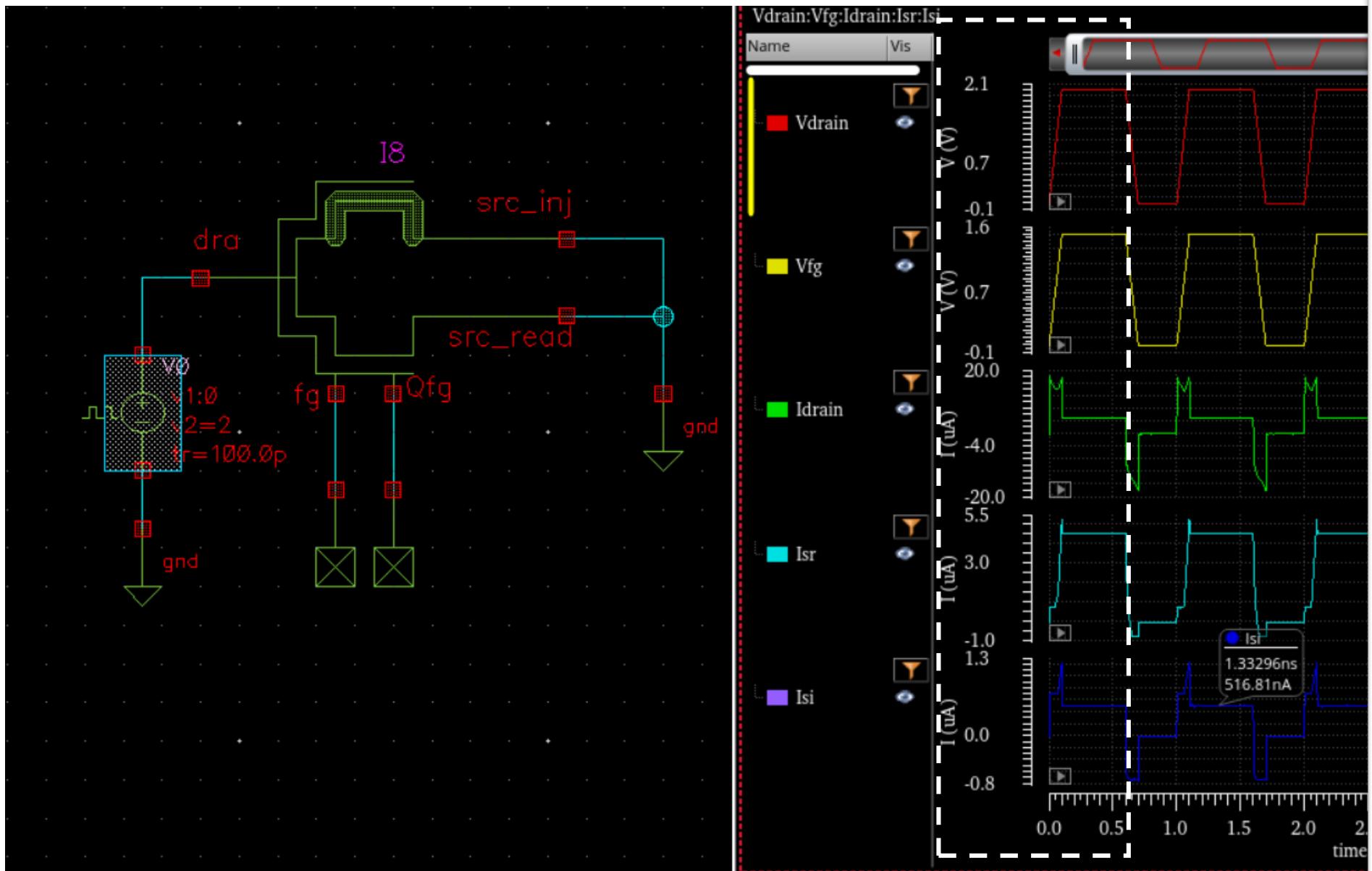


- Data



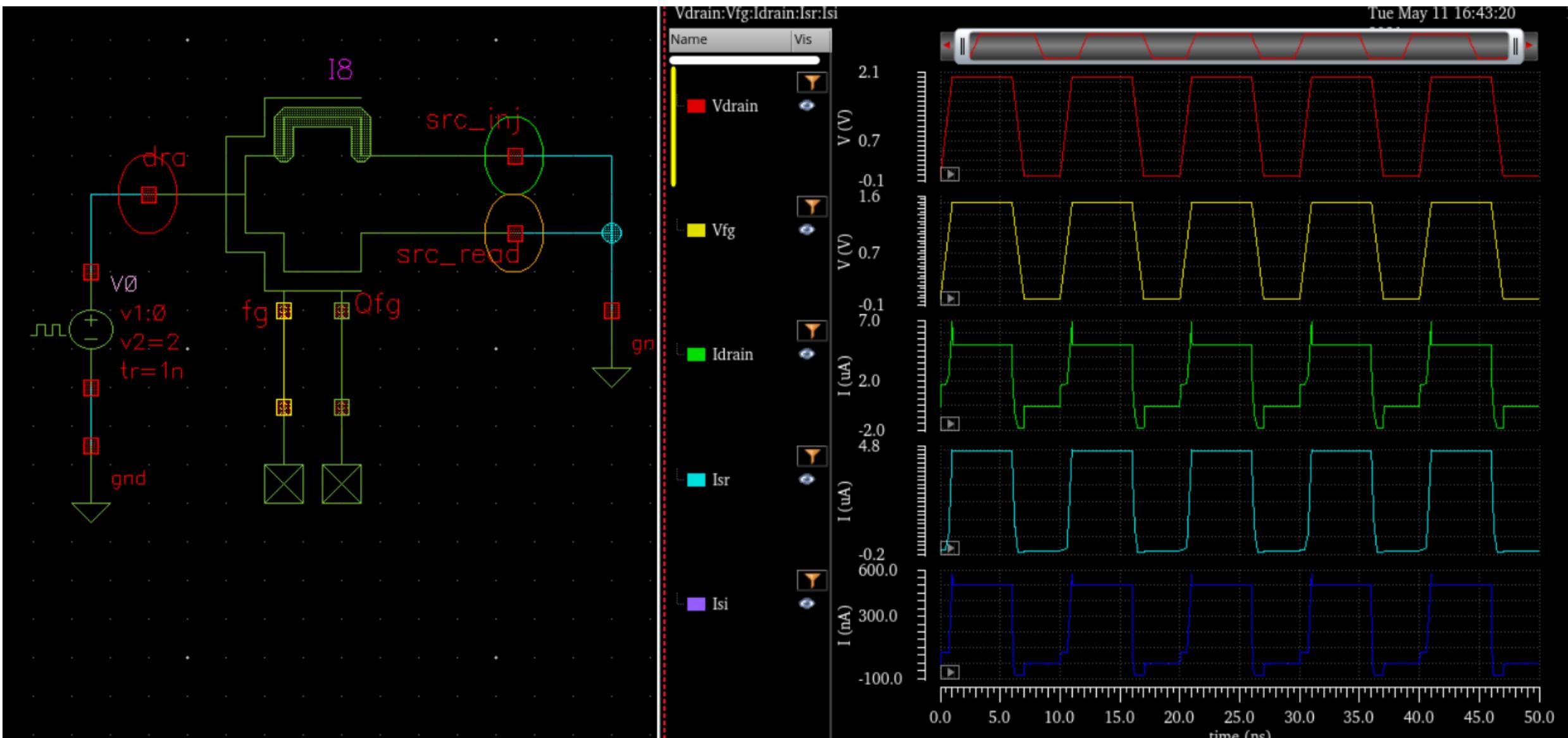
➤ Verilog-a Model Results - 2

- Pulse Reading, tr=0.1ns



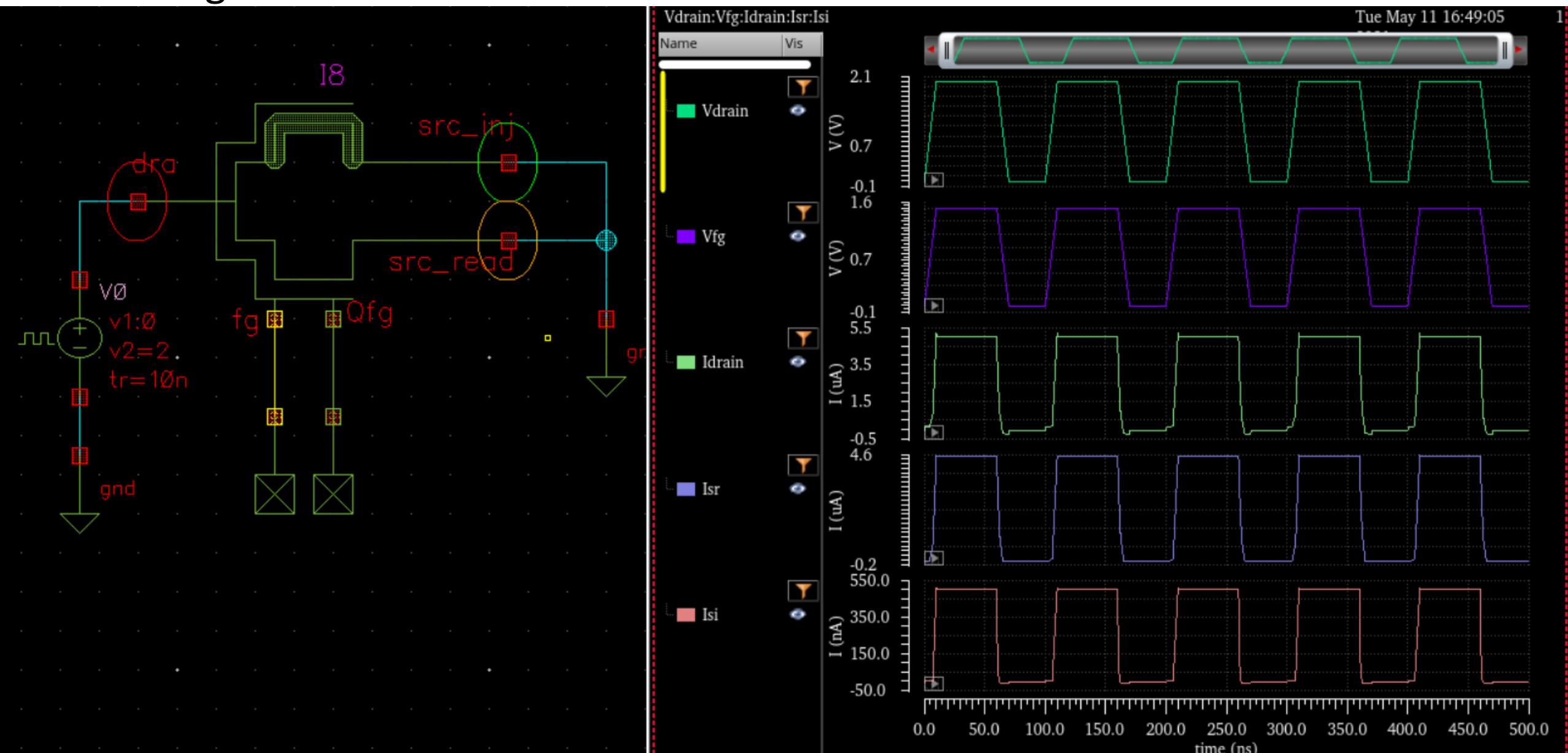
➤ Verilog-a Model Results - 3

- Pulse Reading, tr=1ns



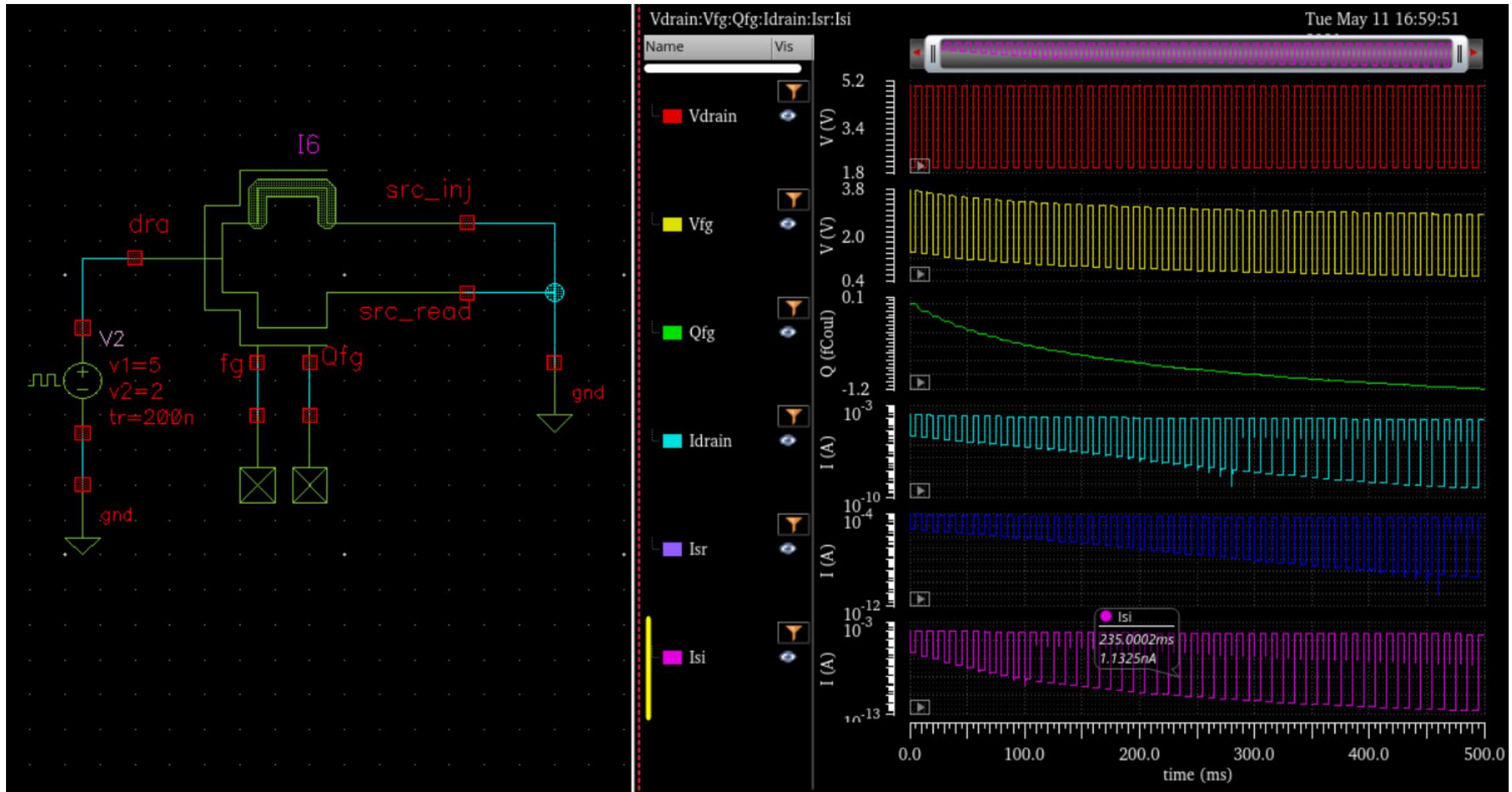
➤ Verilog-a Model Results - 4

- Pulse Reading, tr=10ns



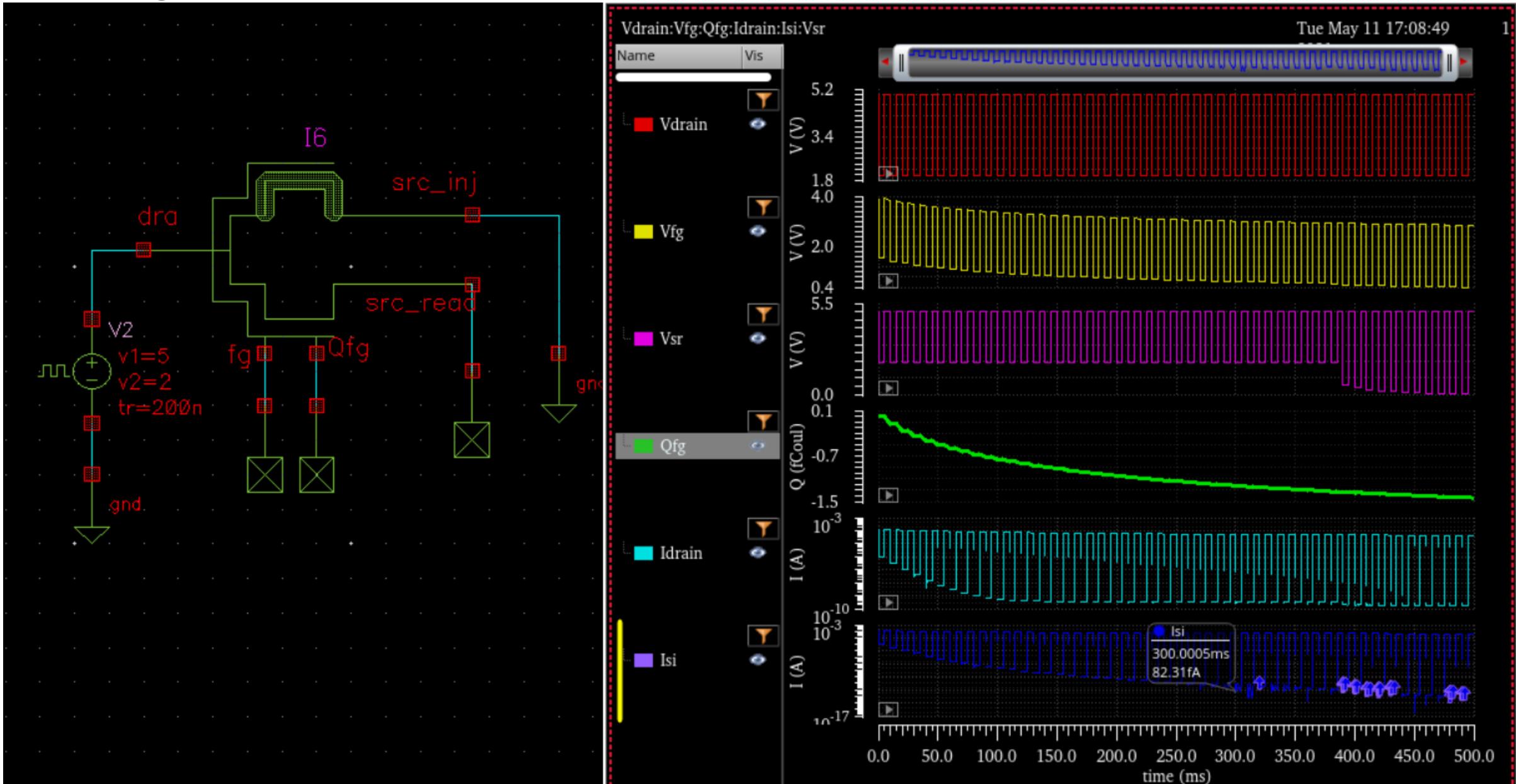
➤ Verilog-a Model Results - 5

- Program, SR shorted with SI



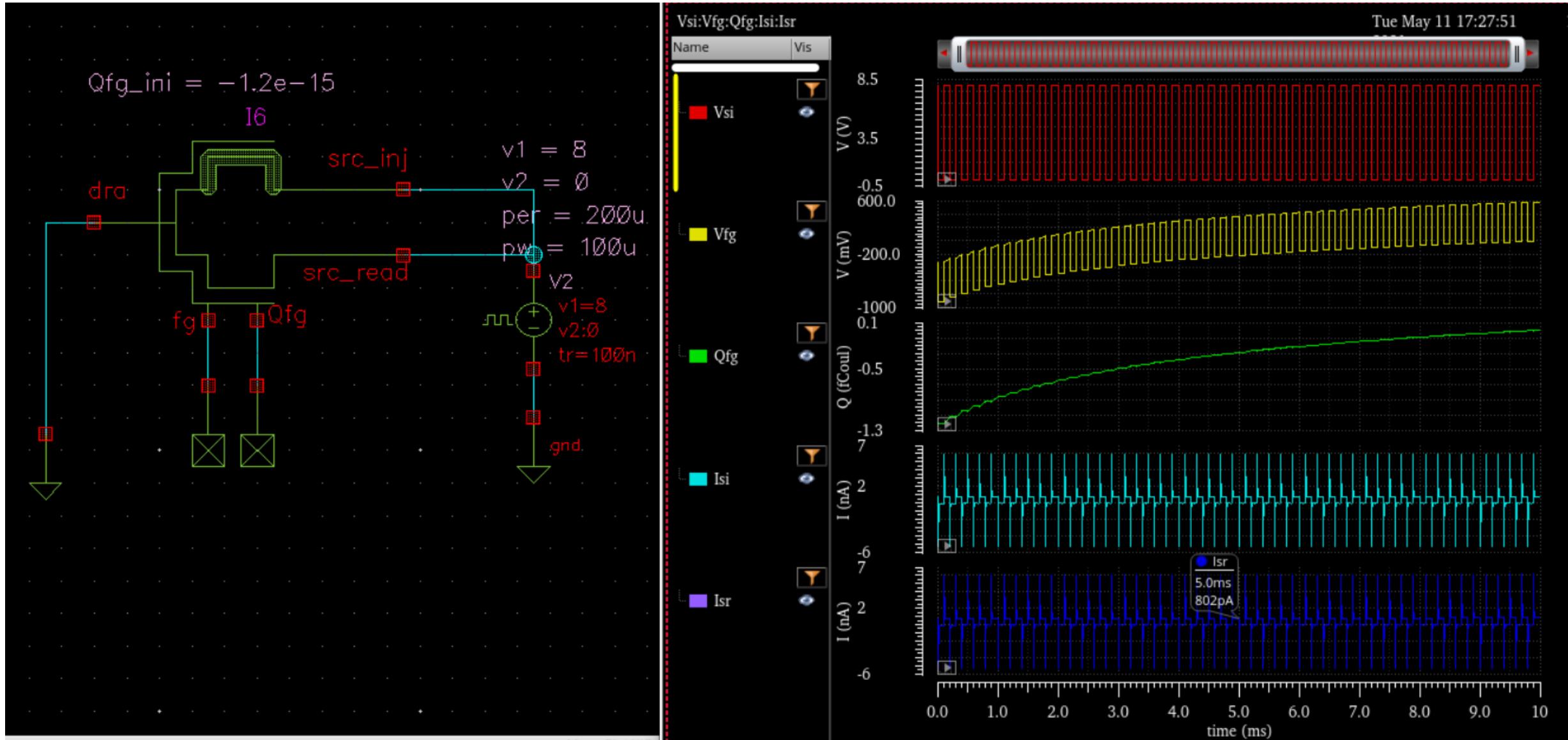
➤ Verilog-a Model Results - 6

- Program, SR floating



➤ Verilog-a Model Results - 7

- Erase, SR shorted to SI



➤ Verilog-a Model Results - 8

- Erase, SR floating

