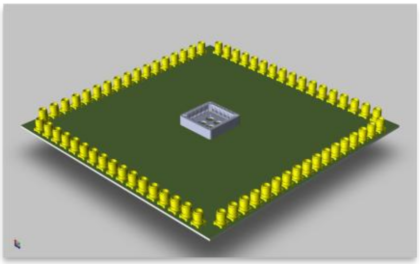
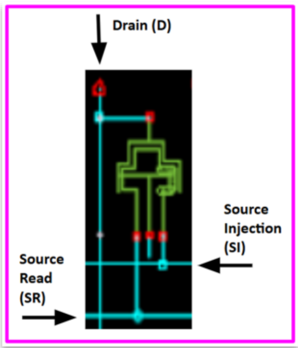
Available !!

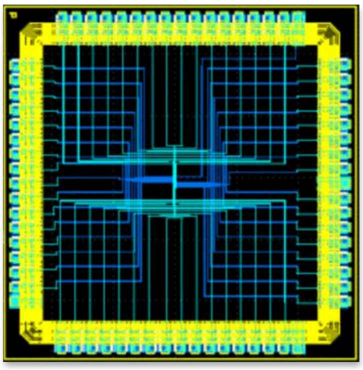
ASIC²
ARCHITECTURES
SYSTEMS
INTELLIGENT COMPUTING
INTEGRATED CIRCUITS

Development of Weight Transfer Scheme for Y-Flash-Based Artificial Neural Network

Recently, several different nonvolatile memory (NVM) technologies, such as NAND Flash, PCM, ReRAM, and STT-MRAM, have emerged as promising candidates for digital and analog in-memory computation. Tower's Y-Flash NVM, fully compatible with standard CMOS process, can be used as a building block which can be used in many artificial neural networks (ANNs) applications owing its multilevel characteristic.
In this project, you develop an experimental setup to write the weights of an ANN to a Y-Flash memory array. This project is part of the NEMO project, where we aim to implement ultra-low-power ANN hardware accelerators.







Project Goals:

In this project, the students will develop a weight transfer scheme for Y-Flash-based ANNs by using an in-house developed board and dedicated lab instruments.

Particularly, students will:

- Learn about the Y-Flash NVM and its use in ANN hardware accelerators.
- Gain practical experience by working with lab instruments including switching matrix and semiconductor device analyzer.
- Develop an efficient and fast writing algorithm that can be experimentally validated at the lab.
- Data analysis according to theoretical terms.
- Write code that controls several measurement equipment simultaneously.

Prerequisites:

- **Courses:** Electronic Circuits or Introduction to VLSI

For more information: ilan.l@technion.ac.il (Ilan Lipschutz)